Configurable Logic Cell (CLC) Configuration Tool User's Guide

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

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For the most up-to-date information on development tools, see the MPLAB® IDE on-line help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the Configurable Logic Cell (CLC) Configuration Tool. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web Site
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the Configurable Logic Cell (CLC) Configuration Tool as a development tool to emulate and debug firmware on a target board. The manual layout is as follows:

- **Chapter 1. CLC Configuration Tool Overview**
- **Chapter 2. Manchester Line Code Example**
- **Appendix A. Manchester Encoding Program (ASSY)**

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at: http://support.microchip.com.

DOCUMENT REVISION HISTORY

Revision A (August 2011)

- Initial Release of this Document.

NOTES:

Chapter 1. CLC Configuration Tool Overview

1.1 INTRODUCTION

The intention of this User's Guide is to assist the reader in becoming acquainted with the Configurable Logic Cell (CLC) Configuration Tool. It will explain how to setup the tool and configure it with an applicable example of creating a Manchester encoder. This document will help the reader become familiar with the purpose and functionality of the CLC module and be able to use the CLC Configuration Tool with ease.

1.2 HIGHLIGHTS

This chapter discusses:

- CLC Configuration Tool Purpose
- Installing the Program
- Configurable Designer Options
- Saving/Loading

1.3 CLC CONFIGURATION TOOL PURPOSE

The CLC consists of multiple combination and sequential circuits that can have their functionality pre-programmed or programmed dynamically. This provides greater flexibility and potential in embedded designs, since the CLC module can operate outside the limitations of software execution and supports a vast amount of output designs.

The configuration tool's purpose is to streamline the setup process of the CLC module by simulating the functionality of the registers in a graphical user interface (GUI). The end result of using the tool will be a generated resource file, written in either C or assembly, which can be dropped into an existing project to be included in a program. The created file is custom generated, depending on the user inputs and preferences, such as programming language.

1.4 INSTALLING THE PROGRAM

The most recent version of the software can be installed from Microchip's web site at http://www.microchip.com. Simply place the `CLCDesignerTool.exe` in the same folder as the `CLCDesigner.ini` file. To run the program, double-click on the executable and the screen in Figure 1-1 should be presented.

FIGURE 1-1: CLC GUI ON INITIAL START-UP

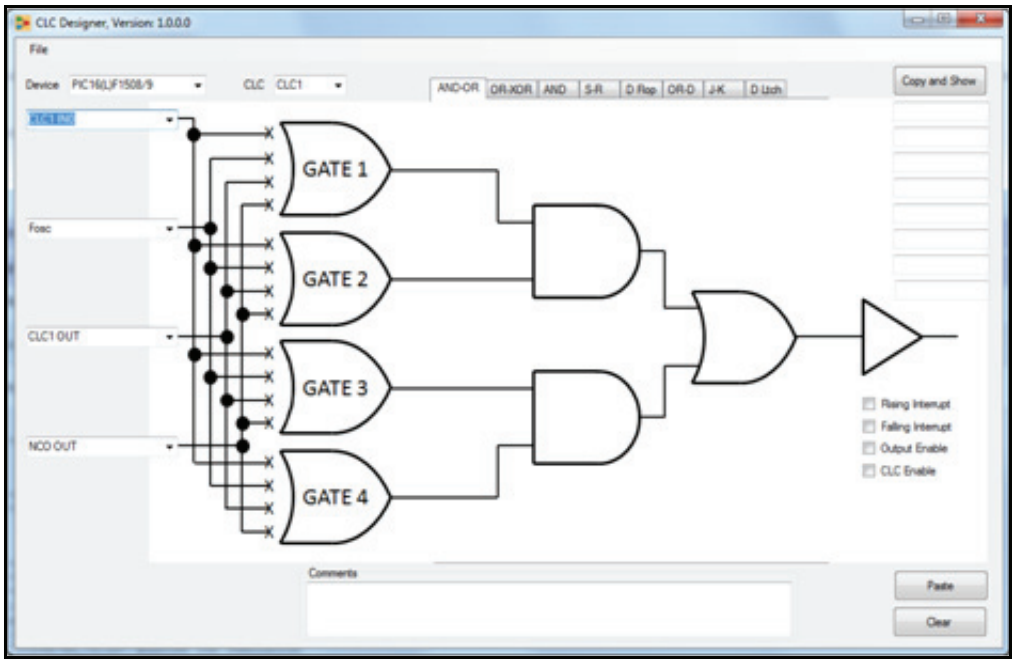
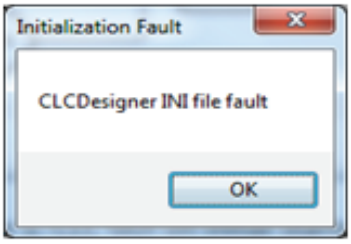


Figure 1-2 shows the error when the INI file is not placed in the same directory as the executable.

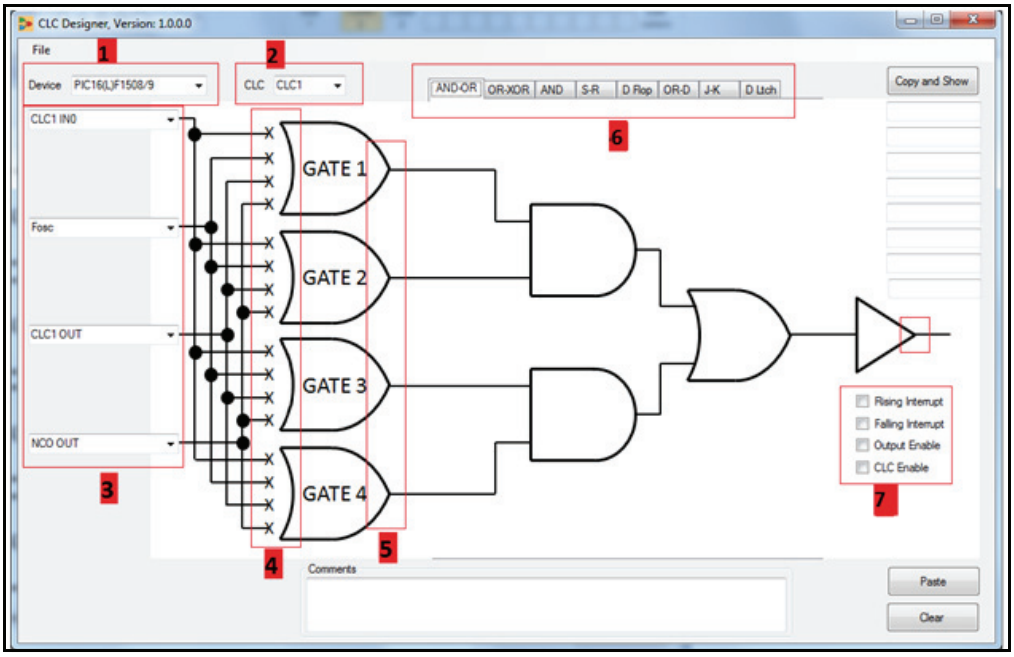
FIGURE 1-2: ERROR MESSAGE



1.5 CONFIGURABLE DESIGNER OPTIONS

The CLC Configuration Tool presents the following options in initial start-up as seen in Figure 1-3.

FIGURE 1-3: CLC INPUT/OUTPUT OPTIONS



The CLC Configuration Tool provides a friendly alternative to manually configuring the 8 CLC registers for each module in software. Table 1-1 correlates each block in the above figure with its matching register in the device's data sheet.

TABLE 1-1: CORRELATION BETWEEN GUI REPRESENTATION AND THEIR EFFECTS ON DATA SHEET CLC REGISTERS

CLC GUI Representation	CLC Registers
1. Device	All
2. CLC module	All
3. Data inputs	CLCxSEL1-2
4. Gate inputs	CLCxGLS1-4
5. Gate output polarity	CLCxPOL
6. Digital logic blocks	CLCxCON
7. CLC output control	CLCxCON

The following sections explains each block's functionality and purpose labeled in Figure 1-3.

1.5.1 Device

This is where the device, such as the PIC16F1508, will be selected. When a device is selected, the program will configure itself automatically to that specific device, such as data inputs and number of available CLC outputs.

1.5.2 CLC Module

This drop-down menu will display each CLC module. Some devices, such as the PIC10F320, will only have one available CLC module in the selected device. The "x" in each CLC register will be replaced by whichever CLC module is used.

1.5.3 Data Inputs

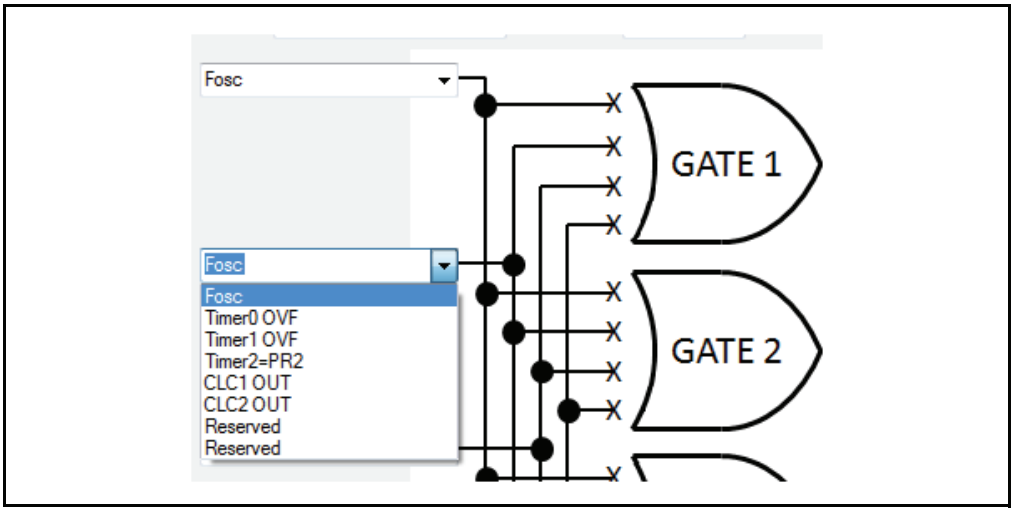
There are four input selection groups. Each group consists of 8 selections. For devices with only 8 inputs, all 8 inputs are available in every group. For devices with 16 inputs, only 8 of the 16 are available in each group but are distributed in such a way to minimize precluding some input selection combinations. No input will appear twice in the same group but will appear as an input in other groups.

As seen in Table 1-2, each drop-down item correlates to a logic cell data input group (lcxdx). Each data input is selectable at least two different times in two or more different groups. For example, FOSC could be selected as an input in the first and second drop-down menus in the CLC tool for a PIC16F1507 as shown in Figure 1-4.

TABLE 1-2: CLCX DATA INPUT SELECTION FOR THE PIC16F1507

Data Input	lcxd1 D1S	lcxd2 D2S	lcxd3 D3S	lcxd4 D4S	CLC1	CLC2
CLCxIN[0]	000	—	—	000	CLC1IN0	CLC2IN0
CLCxIN[1]	001	—	—	101	CLC1IN1	CLC2IN1
CLCxIN[2]	010	—	—	110	Reserved	Reserved
CLCxIN[3]	011	—	—	111	Reserved	Reserved
CLCxIN[4]	100	000	—	—	FOSC	FOSC
CLCxIN[5]	101	001	—	—	TMR0IF	TMR0IF
CLCxIN[6]	110	010	—	—	TMR1IF	TMR1IF
CLCxIN[7]	111	011	—	—	TMR2 = PR2	TMR2 = PR2
CLCxIN[8]	—	100	000	—	CLC1OUT	CLC1OUT
CLCxIN[9]	—	101	001	—	CLC2OUT	CLC2OUT
CLCxIN[10]	—	110	010	—	Reserved	Reserved
CLCxIN[11]	—	111	011	—	Reserved	Reserved
CLCxIN[12]	—	—	100	000	NCO1OUT	LFINTOSC
CLCxIN[13]	—	—	101	001	HFINTOSC	ADCFRC
CLCxIN[14]	—	—	110	010	PWM3OUT	PWM1OUT
CLCxIN[15]	—	—	111	011	PWM4OUT	PWM2OUT

FIGURE 1-4: SELECTION FOSC AS AN INPUT FOR TWO DIFFERENT GATES



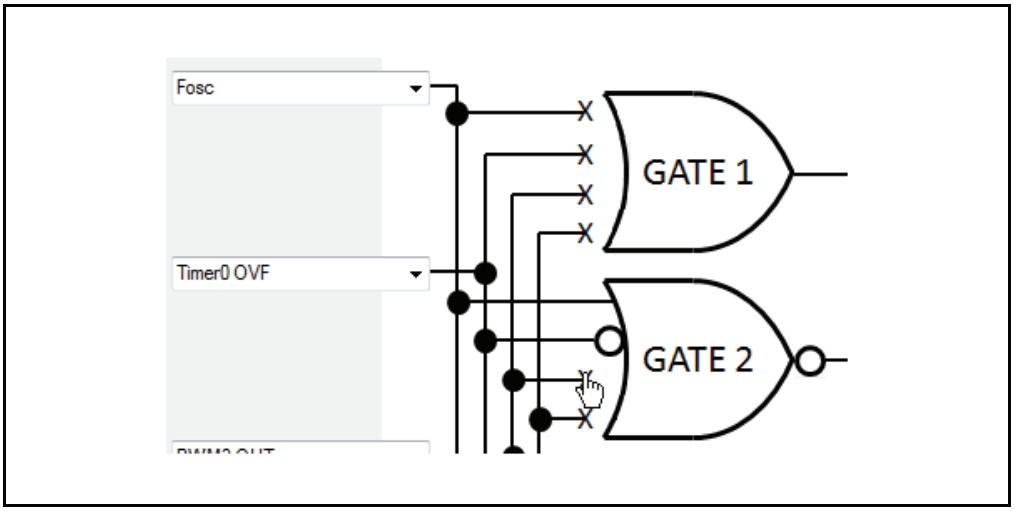
1.5.4 Gate Inputs

Once the data inputs are selected, they can be mapped into each of the four gates. The output of each gate will differ according to the logic function selected. To select an input into a gate, simply hover over the desired “X” and click once. The cursor arrow will have changed to the pointer and a line extending the input into the gate will appear. To invert the signal, click again where the “X” was and now a bubble should appear, indicating an inversion. If clicked once more, the bubble and line should disappear and default back to the original unconnected state.

1.5.5 Gate Outputs

Each of the gate outputs can be inverted. To do so, simply click once on the output of an individual gate for a bubble to appear. The output is now inverted. To undo this, click the bubble again for it to disappear. It is important to note that any gate with no inputs selected will have its output default to the Off state (logic zero). If a constant logic one is desired then invert the default logic zero by clicking the output for the inverting bubble. Figure 1-5 shows the setup of having FOSC and an inverted Timer0 OVF as inputs to Gate 2 with its output inverted.

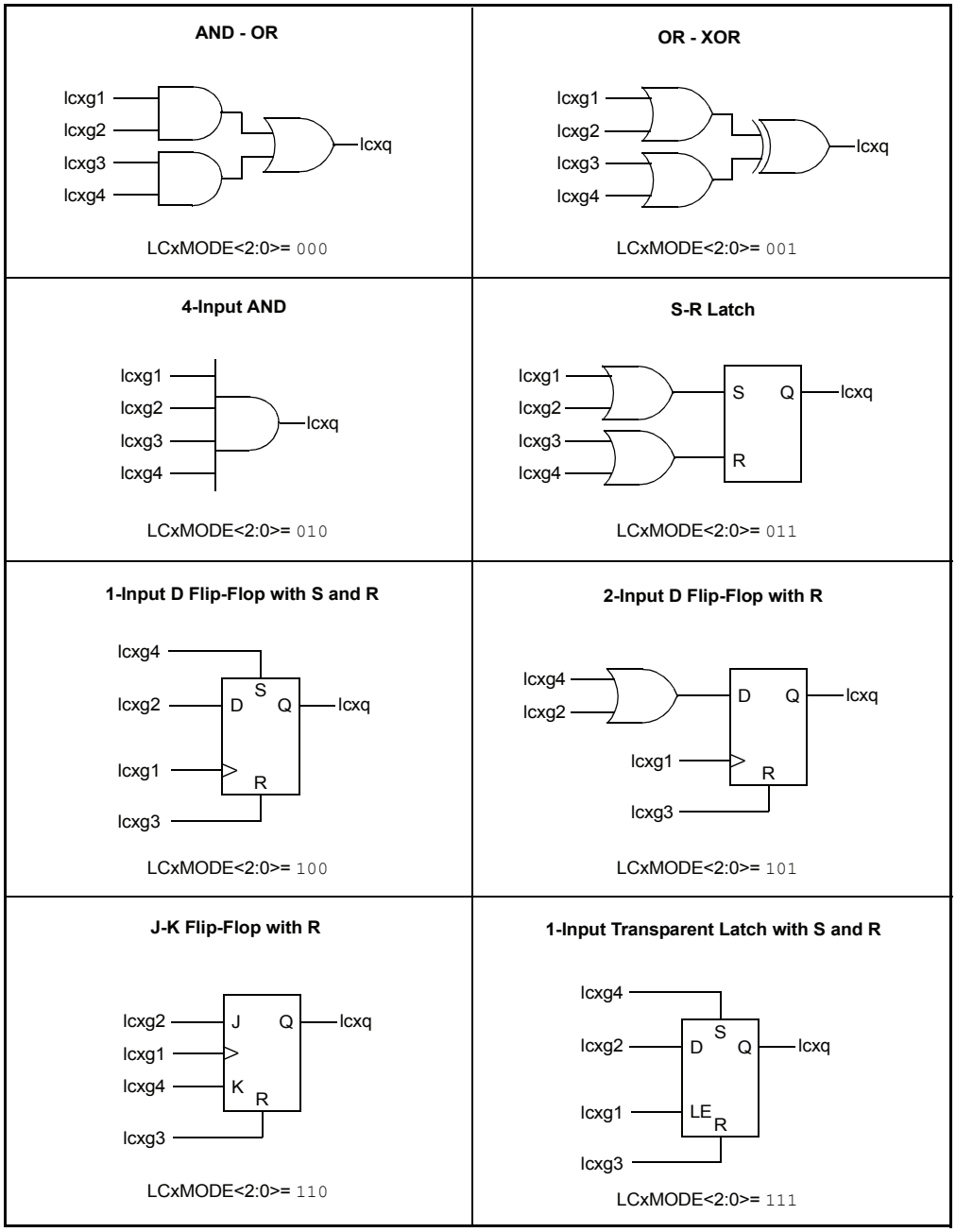
FIGURE 1-5: GATE INPUT/OUTPUT WITH INVERSION



1.5.6 Digital Logic Blocks

There are eight available logic functions selected by the tabs of the CLC tool. The logic blocks cannot be configured other than what is shown. Only one logic function can be used at a single time for each CLC module. Figure 1-6 displays all of the available functions.

FIGURE 1-6: GATE INPUT/OUTPUT WITH INVERSION

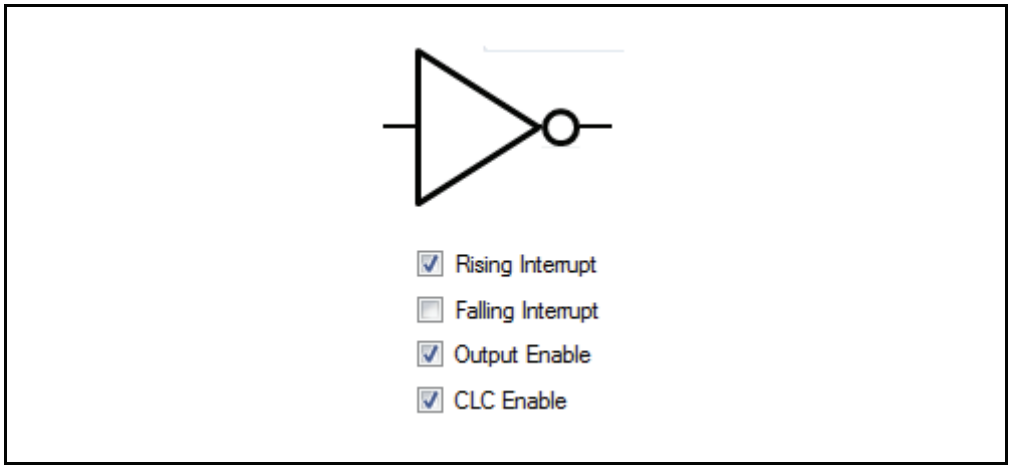


1.5.7 Output Control

The output from the logic block is fed to the last stage of the CLC, the inversion gate. To invert the output, click on the buffer output pin once for a bubble to appear. From here, the output can be routed to other peripherals, an output pin, or back to the CLC input. An interrupt can be enabled upon a rising and/or falling edge from the CLC output.

Figure 1-7 shows the configuration for enabling the module, enabling the output to the CLCx output pin, and producing an interrupt upon a rising edge being detected. The CLC output will also be inverted.

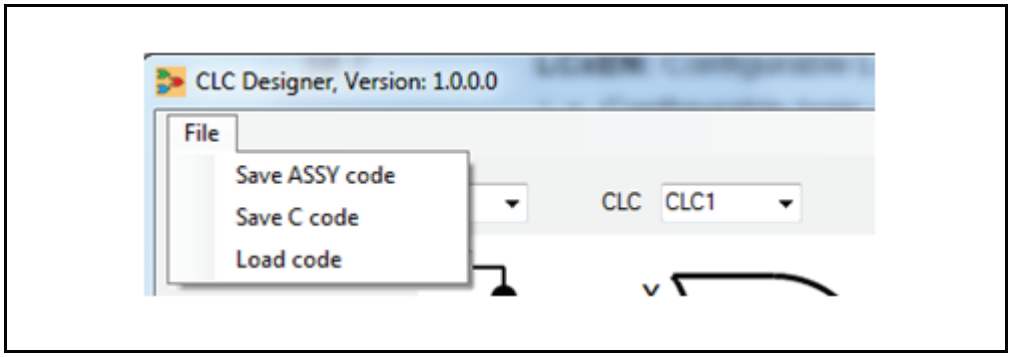
FIGURE 1-7: CLC OUTPUT OPTIONS



1.6 SAVING/LOADING

The program provides convenient methods in saving or loading the design. When the design is concluded and ready to be implemented in software, click the **File** pull-down menu in the top-left corner of the dialog box as shown in Figure 1-8.

FIGURE 1-8: LOCATION OF LOADING AND SAVING CODE IN THE PROGRAM



Then click *file>Save ASSY code* or *Save C code*, depending on the desired output language. The code for all configured CLCs of the selected device will be included in the output file. The resultant file will have an `.inc` extension. Figure 1-7 shows example output code for the setup as seen in Figure 1-6, with the inclusion of the AND-OR logic block and the rest having default settings. The device used in the example is a PIC16F1507 with module CLC1.

EXAMPLE 1-1: EXAMPLE C AND ASSEMBLY GENERATED CODE

```
// File: test.inc
// Generated by CLC Designer, Version: 1.0.0.0
// Date: 7/8/2011 5:51 PM
// Device:PIC16(L)F1507

    CLC1GLS0 = 0x00;
    CLC1GLS1 = 0x06;
    CLC1GLS2 = 0x00;
    CLC1GLS3 = 0x00;
    CLC1SEL0 = 0x14;
    CLC1SEL1 = 0x06;
    CLC1POL  = 0x02;
    CLC1CON  = 0x00;
```

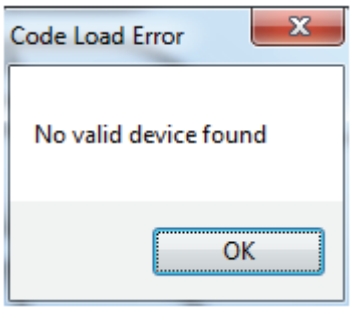
```
; File: test.inc
; Generated by CLC Designer, Version: 1.0.0.0
; Date: 7/8/2011 5:52 PM
; Device:PIC16(L)F1507

    BANKSEL  CLC1GLS0
    movlw    H'00'
    movwf    CLC1GLS0
    movlw    H'06'
    movwf    CLC1GLS1
    movlw    H'00'
    movwf    CLC1GLS2
    movlw    H'00'
    movwf    CLC1GLS3
    movlw    H'14'
    movwf    CLC1SEL0
    movlw    H'06'
    movwf    CLC1SEL1
    movlw    H'02'
    movwf    CLC1POL
    movlw    H'00'
    movwf    CLC1CON
```

Both pieces of code produce the same affect. The assembly is longer due to the nature of the language. The code can now be easily included as a library file or pasted into an existing program. It is important that the comment section is left intact because the CLC tool uses the comments, specifically the device row, to correctly repopulate the fields.

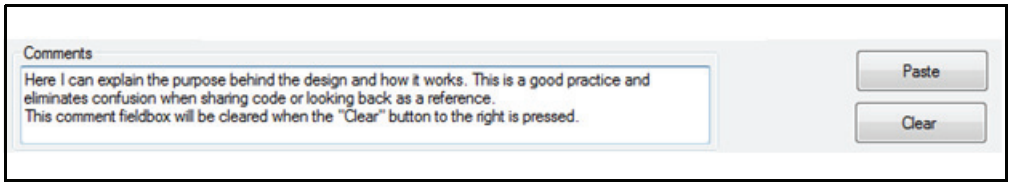
To load previously saved code from the CLC tool, click *file>load code*. If imported successfully, the tool will have populated the GUI with the appropriate values corresponding to the registers in the loaded code. If the message is received as seen in Figure 1-9, the device ID in the comments was deleted and must be put back into place.

FIGURE 1-9: ERROR MESSAGE IF DEVICE ID IS MISSING IN THE COMMENTS OF LOADED CODE



Comments can also be saved and loaded within the output file. To do so, simply fill out the comments input text area as seen in Figure 1-10 and when the project is ready to be saved, the comments will also be included in the output file.

FIGURE 1-10: COMMENT TEXT AREA



The button, **Copy and Show** is used to get a quick view of the register values for the present configuration. When pressed, the boxes below the button will be filled with the settings that correspond to the design. If multiple CLCs share similar configurations, one CLC module can be designed and then pasted into another by clicking the **Copy and Show** in the current module and then **Paste** in another CLC module. This will copy all of the content from one CLC to another. The clipboard contents cannot be pasted to any window outside of the CLC tool. The **Clear** button will reset all fields to their default state.

NOTES:

Chapter 2. Manchester Line Code Example

2.1 INTRODUCTION

This example will use the information in **Chapter 1. "CLC Configuration Tool Overview"** in solving a typical problem that can now be achieved with ease using the Configurable Logic Cell Configuration Tool. It is recommended that the reader first understand how to use the program before continuing.

2.2 HIGHLIGHTS

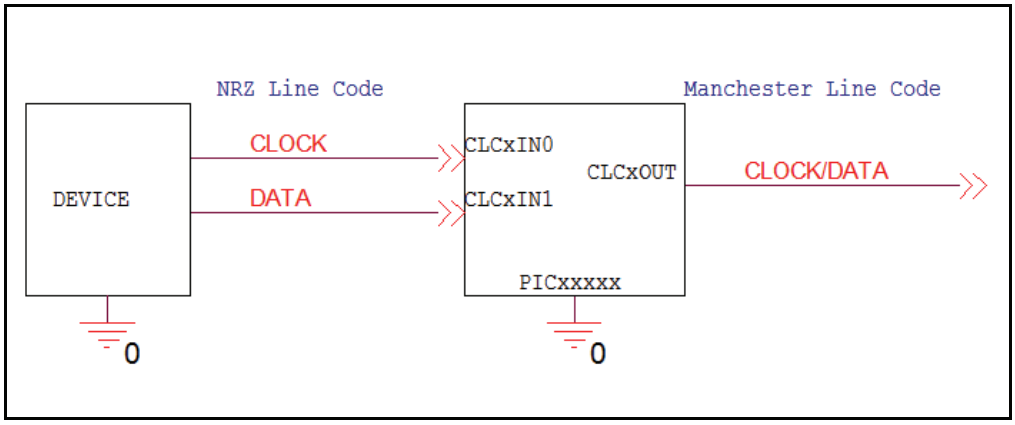
This chapter discusses:

- Example Problem
- Proposed Solution
- Extended Solution

2.3 EXAMPLE PROBLEM

You want to encode a bit stream of a typical non-return-to-zero (NRZ) line code from a certain device to a slimmer, more versatile Manchester line code. A Manchester line code has advantages over the typical NRZ code in that Manchester encoding combines the clock and data into one data stream. It has no DC component and is self-clocking. A diagram of a potential setup is shown in Figure 2-1.

FIGURE 2-1: NRZ LINE CODE ENCODED TO A MANCHESTER CODE



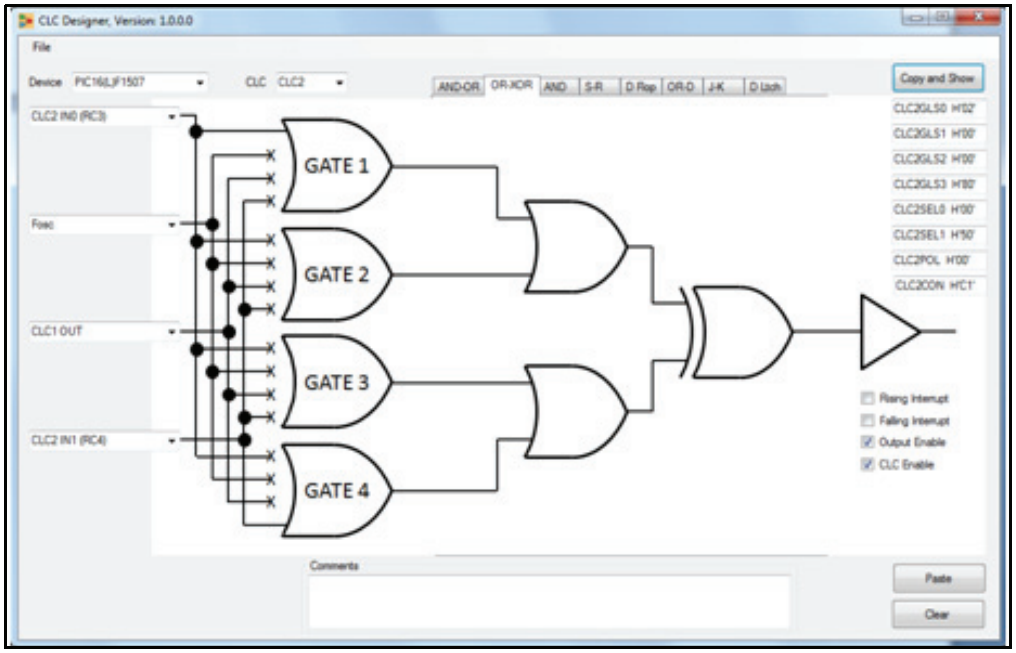
2.4 PROPOSED SOLUTION

Using only one CLC module on a PIC® device would accomplish this task. There would be no limitation to the clock speed, since the CLC is not controlled by software. This allows the CPU to focus on the main program without dealing with the encoding process. This also saves the designer additional costs by not having to include more external hardware to perform the same task.

The encoding process simply requires an XOR gate with the data and clock inputs. For this design, a PIC16F1507 is used with its CLC2 module.

The data and clock are mapped to CLC2s input on RC3 and RC4, respectively. It is vital that their respective TRIS bits are configured as inputs. Enable the CLC output and the module itself as well as clear the TRIS bit for the CLC output pin. Figure 2-2 shows the CLC design.

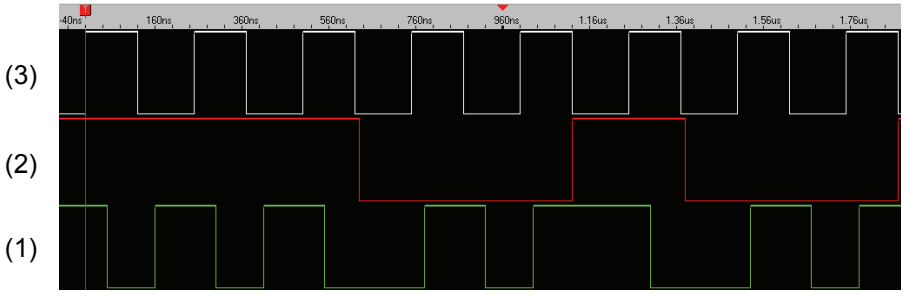
FIGURE 2-2: CLC DESIGN FOR THE ENCODE HANDLING



When finished, include a short description in the comment box and save the design in either C or Assembly format. See **Appendix A. "Manchester Encoding Program (ASSY)"** for the source code in Assembly.

Figure 2-3 shows a screenshot of the output of the CLC, assuming an input of 0xE4 from the device.

FIGURE 2-3: MANCHESTER LINE ENCODING FROM AN NRZ SOURCE USING THE CLC

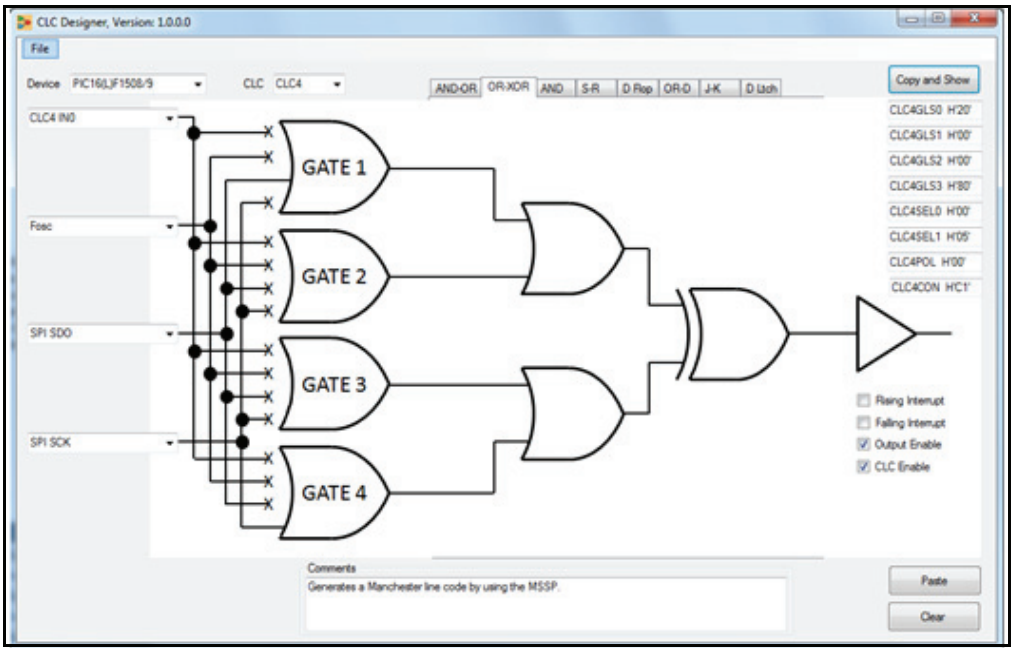


Note: Green = CLC output (1), Red = data (2), White = clock (3).

2.5 EXTENDED SOLUTION

If the user wants to generate a Manchester encoded message from the PIC device directly, this is easily achieved through the MSSP. Simply select the PIC16F1508 and replace the data/clock inputs from the external device with SPI SCK and SPI SDO.

FIGURE 2-4: CLC DESIGN FOR THE ENCODE HANDLING USING THE MSSP AS INPUTS



Note: See **Appendix A. "Manchester Encoding Program (ASSY)"** for assembly code solution.

NOTES:

Appendix A. Manchester Encoding Program (ASSY)


```
#include "p16f1507.inc"

    __CONFIG _CONFIG1, _FOSC_INTOSC & _WDTE_OFF & _PWRTE_OFF &
_CLKOUTEN_OFF
    __CONFIG _CONFIG2, _LVP_OFF & _STVREN_ON   ;Stack over/under flow
will cause a reset

    errorlevel -302      ;suppress bank selection not zero warning


    ORG 0x00

main
    call      main_init  ;init CLC and configure PIC inputs/outputs
    goto      main_loop  ;main waiting loop
main_loop
    goto      main_loop  ;sit here forever

main_init
; File: clc.inc
; Generated by CLC Designer, Version: 1.0.0.0
; Date: 7/13/2011 12:44 PM
; Device:PIC16(L)F1507

    BANKSEL  CLC1GLS0
    movlw  H'00'
    movwf  CLC1GLS0
    movlw  H'00'
    movwf  CLC1GLS1
    movlw  H'00'
    movwf  CLC1GLS2
    movlw  H'00'
    movwf  CLC1GLS3
    movlw  H'00'
    movwf  CLC1SEL0
    movlw  H'00'
    movwf  CLC1SEL1
    movlw  H'00'
    movwf  CLC1POL
    movlw  H'00'
    movwf  CLC1CON
```

```
    BANKSEL  CLC2GLS0
    movlw  H'02'
    movwf  CLC2GLS0
    movlw  H'00'
    movwf  CLC2GLS1
    movlw  H'00'
    movwf  CLC2GLS2
    movlw  H'80'
    movwf  CLC2GLS3
    movlw  H'00'
    movwf  CLC2SEL0
    movlw  H'50'
    movwf  CLC2SEL1
    movlw  H'00'
    movwf  CLC2POL
    movlw  H'C1'
    movwf  CLC2CON

;Uses CLC2out
    banksel   OSCCON
    movlw     b'01110010';8MHz clock - Does not matter for this demo
    movwf     OSCCON
    banksel   TRISC
    movlw     b'10011000'; RC3 & RC4 as input to CLC2IN :: RC0 as
output form CLC2
    movwf     TRISC
    banksel   ANSELC     ;All digital outputs
    movlw     0x00
    movwf     ANSELC

    return               ;return to main program
```

NOTES:

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