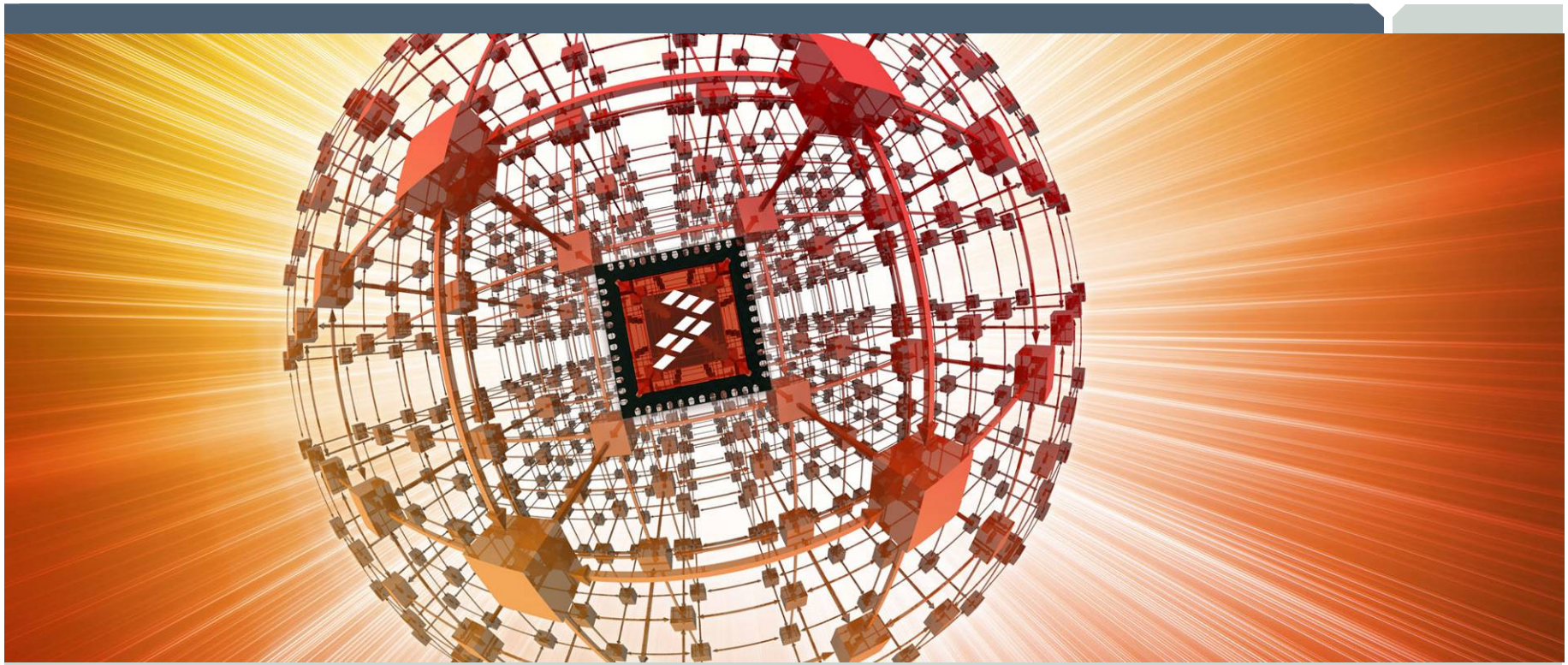

DwF 2011

Kinetis ARM® Cortex™-M4 Microcontrollers

Stefan Imrich
Field Application Engineer

Matthias Ackermann
Field Application Engineer

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Freescale MCU & MPU - Product Overview

32-bit	***Built on…*** **Power Architecture® Technology**	90nm	100-400+ MIPS	Market-leading performance, reliability and software enablement for automotive and industrial applications.
	Kinetis *based on ARM® Cortex™-M4 core*	NEW! 90nm	50-200 MIPS	Scalable, ultra-low-power product families with bundled software enablement for industrial and consumer applications.
	ColdFire ColdFire+	NEW! 90nm	50-200 MIPS	Application-oriented ultra-low power solutions with optimized enablement, integration and cost for appliance, metering and consumer applications.
16-bit	**Digital Signal Controllers S12 and S12X**			Application-oriented solutions for automotive, motor control and power conversion applications.
8-bit	**RS08 and S08**			Scalable cost & power-optimized product families for industrial, automotive and consumer applications.

Giving customers an ideal solution regardless of architecture preference.

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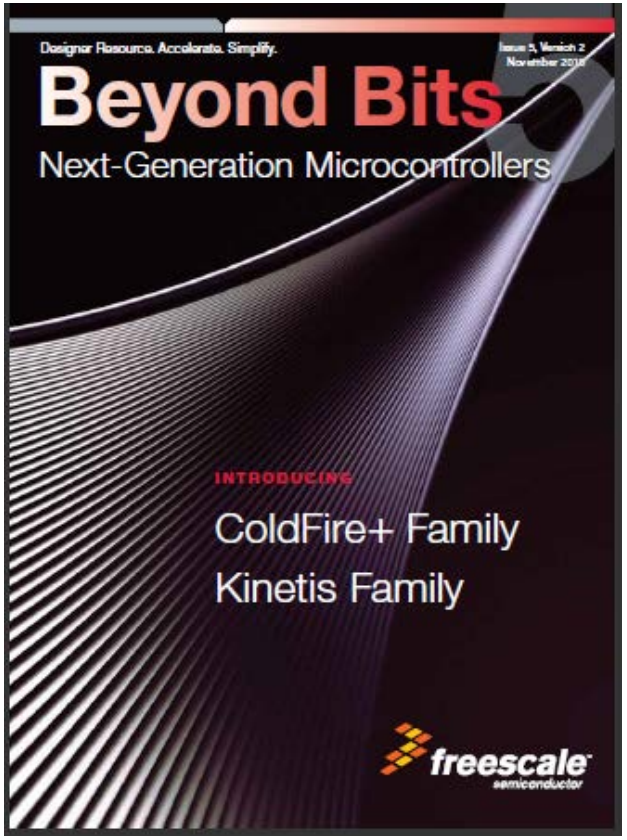
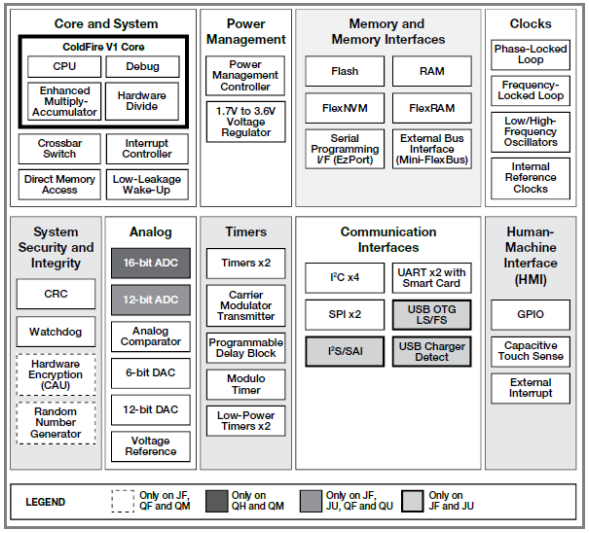
Freescale ColdFire+ and Kinetis - Product Overview

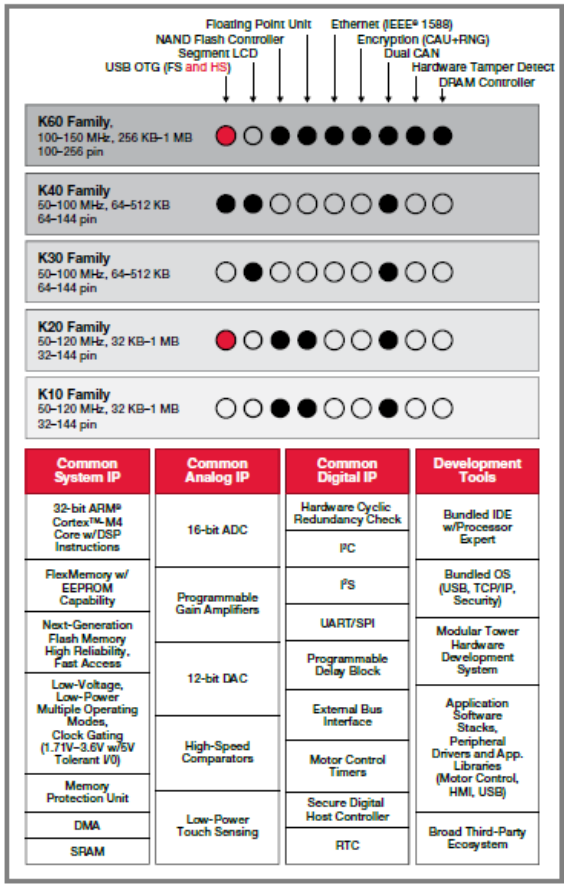
http://www.freescale.com/BeyondBits



ColdFire+



Kinetis



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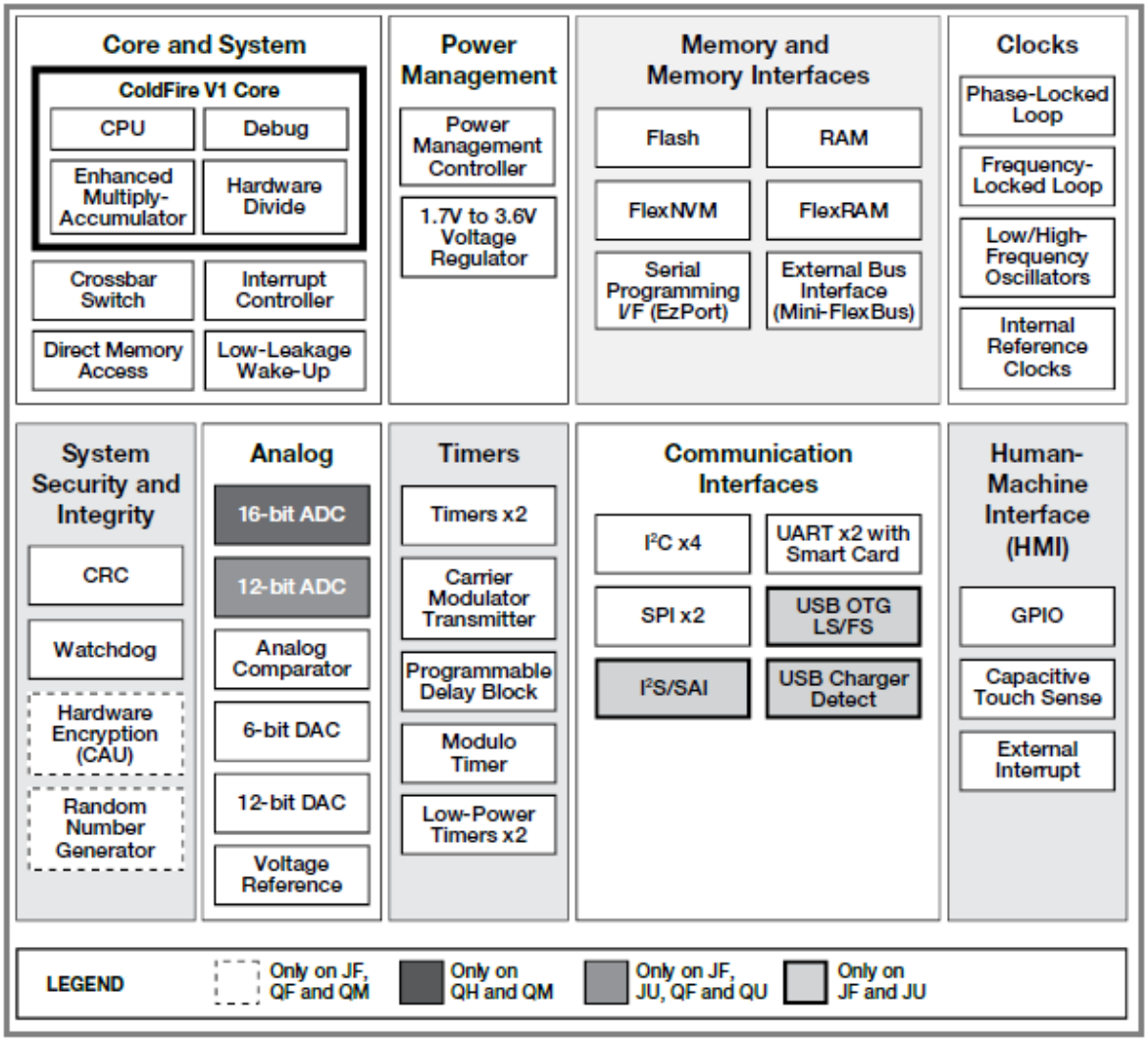
Freescale ColdFire+



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Expanding Freescale's Extensive 32-bit Solutions Portfolio

Market-leading software enablement – IDE, RTOS and initialization tools from Freescale and leading ARM ecosystem providers to speed time to market

Innovative low-power **90nm thin film storage flash** process with **FlexMemory** EEPROM capability

Hundreds of new 32-bit mixed-signal MCUs with huge **performance**, **memory** and **feature scalability**

Ultra-low power consumption with flexible power management to balance performance and battery life

More than 240 new 90nm 32-bit MCUs in scalable product families

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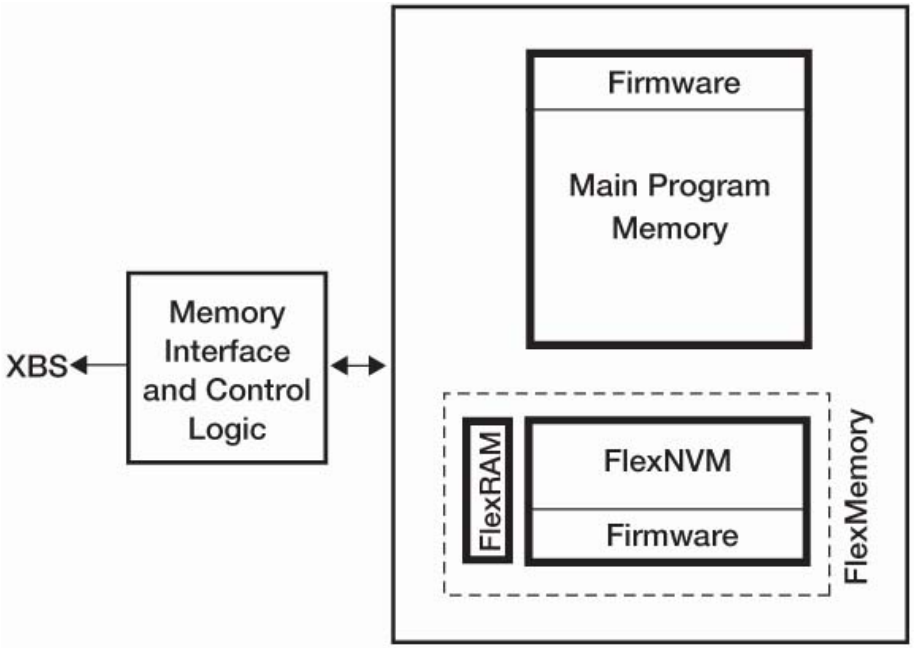
90nm Thin Film Storage with FlexMemory Technology

90nm Thin Film Storage: split-gate non-volatile memory

Freescale's 90nm Thin Film Storage (TFS) flash memory technology with FlexMemory will deliver outstanding performance, value, reliability and low power for next generation industrial and consumer microcontrollers.

www.freescale.com/TFS

- Industry leading bit-level reliability through revolutionary silicon nanocrystal technology
- Fast, low-voltage transistors that provide low-power read capability and help satisfy the increasing demands of power-sensitive applications with full flash operation specified down to 1.71 volts
- Flash access times of >30 nanoseconds; and excellent area efficiency, enabling a rich level of memory and peripheral integration across flash densities, while maintaining optimal MCU cost



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90nm Thin Film Storage with FlexMemory Technology

90nm Thin Film Storage: split-gate non-volatile memory

Attribute	Traditional Embedded EEPROM	FlexMemory
Read-while-write with program memory	Yes	Yes
Granularity	Byte write/erase	Byte write/erase
Write time	~1-5msec (byte write only)	~100usec (word or byte program, brown-outs w/o loss or corruption of data)
Erase + write time	~5-10 msec	~750 usec + ~750 usec (1.5 msec)
Guaranteed endurance	50-300K cycles (fixed)	SoC implementation and user configurable, can exceed 10M cycles
Minimum write voltage	≥ 2.0V	1.71V
Flexibility	Fixed by part number	Programmable trade-off - quantity vs. endurance

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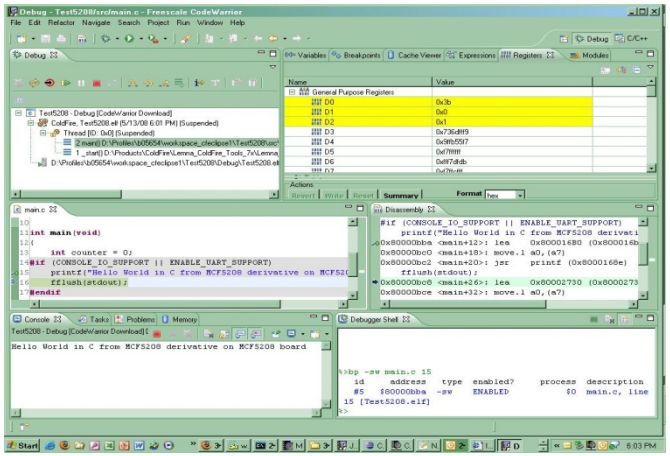
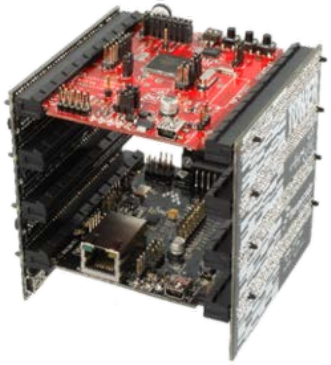
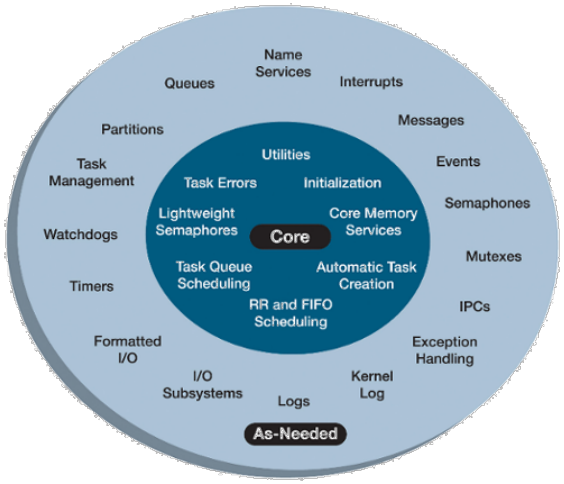
Freescale Tools Support



CodeWarrior v10.x (*Eclipse IDE*) and ProcessorExpert



Tower System



MQX System

ColdFire+ *and Kinetis solutions are supported by Freescale's industry-leading software* enablement – CodeWarrior, MQX™ and Processor Expert

See for 'CodeWarrior Development Studio for Microcontrollers v10.0 (Eclipse)' >> http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=CW-MCU10&tid=CWH

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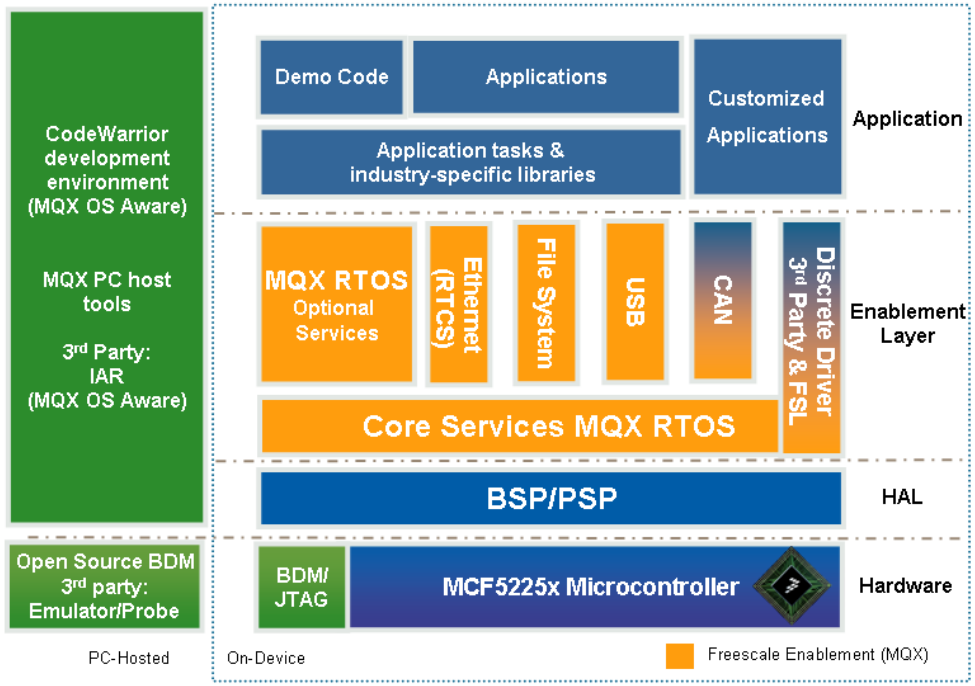
Freescale MQX RTOS

www.freescale.com/MQX

What is FSL MQX?

- ✓ *RTOS (Full priority-based, pre-emptive scheduler)*
- ✓ *Real-time TCP/IP Com. Suite [TCP/IP, FTP, Telnet, DHCP, SNMP etc.]*
- ✓ *USB Host - HID, MASS, HUB*
- ✓ *USB Device - HID, MASS, CDC*
- ✓ *MS-DOS File System (MFS)*
- ✓ *PC Host Tools*
- ✓ *BSP I/O Driver: CAN, UART etc…*
- ✓ *HTTP Web server*



Highlights

Customers get access to source code, & can edit source code (*remain with customer*).

Fully optimized, integrated, tested, & configurable with our MCUs, Demo boards and CodeWarrior.

MQX is approved for use in Medical & Aerospace applications, & been in industry for 15years.

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Freescale MQX RTOS

Add-on Software, & Features

www.freescale.com/MQX

Freescale MQX™ Add-on Software

Other Freescale MQX products are pre-integrated by a broad ecosystem of Freescale Alliance members. If you cannot find the protocols you require, please contact our partners, for up to date information.

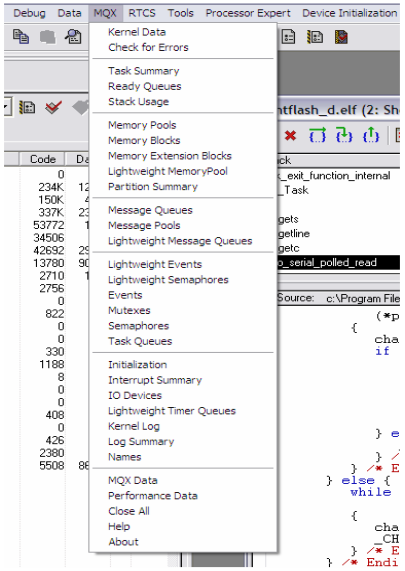
Available Pre-Integrated Software:

- 802.11b Wi-Fi Software Module
- Real-Time TCP/IP Communication Suite (RTCS) Optional Components
- Network Security Protocols
- PEG+ Graphics Library
- SEGGER emWin Graphics Library/GUI
- CANopen Master/Slave for Embedded Devices
- Industrial Network and Field Bus Protocols
- SFFS Flash File System
- ...
- *Freescale eGUI (Driver for Display)*

Task-Aware Debugging (TAD)

Supported with CW Professional Suite:

- ✓ Task Summary Display
- ✓ Task Stacks Display
- ✓ Task Semaphore Display
- ✓ Task Ready List Display
- ✓ Tasks Queues Display
- ✓ Memory Pools Display
- ✓ Memory Blocks Display
- ✓ Memory Partitions Display
- ✓ Semaphore Display
- ✓ Mutexes Display
- ✓ Events Display
- ✓ Logs Display
- ✓ IO Devices Display
- ✓ Interrupts Display



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New Kinetis MCUs

ARM® Cortex™-M4 MCUs

Cortex-M4(F) new features

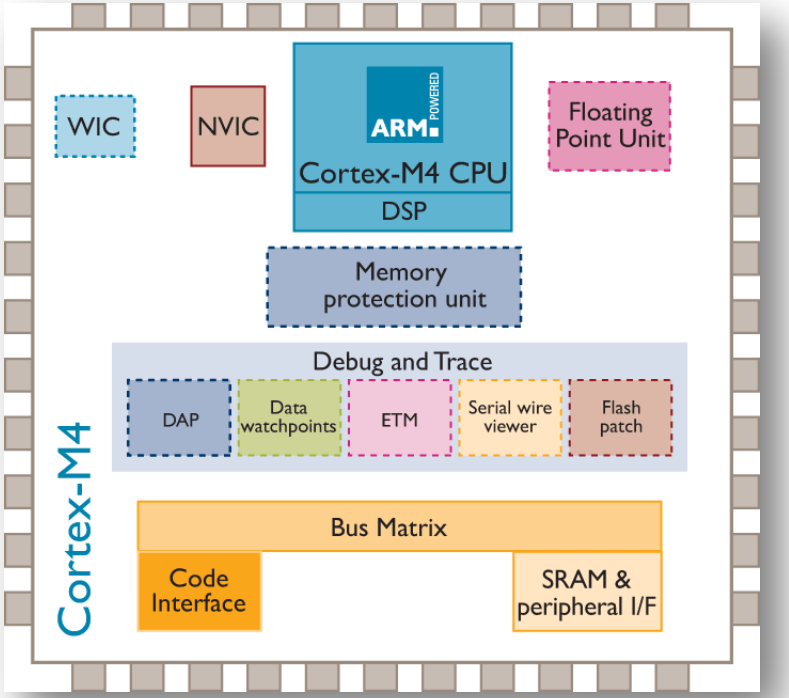
- ✓ Single cycle MAC (Up to 32 x 32 + 64 -> 64)
- ✓ DSP extensions by default
- ✓ Single Precision Floating Point Unit (*optional*)

Freescale IP and Innovation

- ✓ On-chip instructions / data cache (*optional*)
- ✓ Cross-Bar Switch (concurrent multi-master/slave access)
- ✓ On-chip DMA for CPU off-load
- ✓ Low-leakage Wake-up (*in addition to AWIC*) Unit

Freescale IP for Digital Signal Processing

- ✓ Motor Control:
  Advanced algorithms, longer lifespan, power efficiency
- ✓ Automation
  High calculation and algorithm bandwidth at a low cost
- ✓ Power management
  Designed for low/battery powered systems
- ✓ Audio and Video
  5x performance improvement over software, making batteries last longer



Backwards compatible with ARM Cortex-M3

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New Kinetis MCUs - Signal Processing

ARM® Cortex™-M4 MCUs

CLASS	INSTRUCTION	ARM9E-S	CORTEX-M3	CM4
Arithmetic	ALU operation (not PC)	1 - 2	1	1
	ALU operation to PC	3 - 4	3	3
	CLZ	1	1	1
	QADD, QDADD, QSUB, QDSUB	1 - 2	n/a	1
	QADD8, QADD16, QSUB8, QSUB16	n/a	n/a	1
	QDADD, QDSUB	n/a	n/a	1
	QASX, QSAX, SASX, SSAX	n/a	n/a	1
	SHASX, SHSAX, UHASX, UHSAX	n/a	n/a	1
	SADD8, SADD16, SSUB8, SSUB16	n/a	n/a	1
	SHADD8, SHADD16, SHSUB8, SHSUB16	n/a	n/a	1
	UQADD8, UQADD16, UQSUB8, UQSUB16	n/a	n/a	1
	UHADD8, UHADD16, UHSUB8, UHSUB16	n/a	n/a	1
	UADD8, UADD16, USUB8, USUB16	n/a	n/a	1
	UQASX, UQSAX, USAX, UASX	n/a	n/a	1
	UXTAB, UXTAB16, UXTAH	n/a	n/a	1
	USAD8, USADA8	n/a	n/a	1
Multiplication	MUL, MLA	2 - 3	1 - 2	1
	MULS, MLAS	4	1 - 2	1
	SMULL, UMULL, SMLAL, UMLAL	3 - 4	5 - 7	1
	SMULBB, SMULBT, SMULTB, SMULTT	1 - 2	n/a	1
	SMLABB, SMLBT, SMLATB, SMLATT	1 - 2	n/a	1
	SMULWB, SMULWT, SMLAWB, SMLAWT	1 - 2	n/a	1
	SMLALBB, SMLALBT, SMLALTB, SMLALTT	2 - 3	n/a	1
	SMLAD, SMLADX, SMLALD, SMLALDX	n/a	n/a	1
	SMLSD, SMLSDX	n/a	n/a	1
	SMLSLD, SMLSLD	n/a	n/a	1
	SMMLA, SMMLAR, SMMLS, SMMLSR	n/a	n/a	1
	SMMUL, SMMULR	n/a	n/a	1
	SMUAD, SMUADX, SMUSD, SMUSDX	n/a	n/a	1
	UMAAL	n/a	n/a	1
Division	SDIV, UDIV	n/a	2 - 12	2 – 12

Cortex-M4 Single cycle MAC

Kinetis Benchmark:
EEMBC CoreMark Code as a point of comparison. Result <1.3 CPU cycles per flash access (< 0.3 wait states) @100 MHz.

This approaches 1cycle/access as the core frequency approaches 50 MHz.

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New Kinetis MCUs - Math & DSP Library

ARM® Cortex™-M4 MCUs

Complimentary Math and DSP Library including:

- ✓ C callable and operating system independent functions
- ✓ Functions optimized for ARM Cortex-M4 using compiler intrinsics for DSP/SIMD instructions
- ✓ Separate functions for 8-bit, 16-bit, 32-bit integers and 32-bit floating-point values
- ✓ Supports many math and DSP functions:

Filtering
- ✓ Biquad cascade direct form 1 (IIR)
- ✓ Convolution
- ✓ Partial convolution
- ✓ FIR (transversal) filter
- ✓ Polyphase FIR decimator
- ✓ Polyphase FIR interpolator
- ✓ LMS adaptive filter
- ✓ Normalized LMS adaptive filter
- ✓ Sparse FIR filter
- ✓ Correlation
- ✓ 64-bit high precision biquad filters
- ✓ FIR lattice filters
- ✓ Direct form 2 transposed IIR filter
- ✓ IIR lattice filters

Transforms
- ✓ Complex forward FFT
- ✓ Real FFT
- ✓ Inverse real FFT
- ✓ Discrete cosine transform
- ✓ Inverse discrete cosine transform

Matrix addition, subtraction, transpose, scaling, inversion

Controller
- ✓ PID controller
- ✓ Field oriented control (clarke and park transforms)

Vector Math
- ✓ Absolute value
- ✓ Add (element by element)
- ✓ Vector dot product
- ✓ Multiply elements
- ✓ Invert sign (negate)
- ✓ Add constant offset
- ✓ Scale by constant
- ✓ Shift left/right
- ✓ Subtract (element by element)

Fast Math
- ✓ Sine, Cosine, Square root

Interpolation (linear and bilinear)

Complex Math
- ✓ Complex conjugate
- ✓ Complex magnitude
- ✓ Complex magnitude squared
- ✓ Complex by complex multiplication
- ✓ Complex by real multiplication
- ✓ Complex dot product

Statistics
- ✓ Maximum / minimum value
- ✓ Mean
- ✓ Power
- ✓ Root mean square (RMS)
- ✓ Standard Deviation
- ✓ Variance

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New Kinetis MCUs - Signal Processing

ARM® Cortex™-M4 MCUs

Audio improvements using Cortex-M4

- ✓ **Core loop cycle advantage of 4x to 8x**
  - Mixed bit width arithmetic (DSP instruction)
  - Packed processing with SIMD
- ✓ **Registers usage is comparatively less**
- ✓ **Overall cycle advantage of approximately 2x**
- ✓ **Lesser code size further improves performance**

Example	Cortex-M4 speed vs. M3
Audio – Window Overlap and Add	1.8x – 2.6x faster
FIR Filter	2x faster
MP3 Decoder	2x faster
WMA Decoder	1.6x faster
Motor Control – Clarke Transform	5x faster
Motor Control – Park's Transform	7x faster

Motor Control using Cortex-M4

- ✓ **New DSP oriented instructions enable a new level of sophistication in sensorless control**
  - Faster control loops – more responsive to speed commands and changing loads
  - More sophisticated estimators for sensorless control

Cortex-M4 energy efficiency

- ✓ **Chip can be clocked at half (or less) the MHz of Cortex-M3 to accomplish same workload**
- ✓ **Leads to longer battery life and higher energy efficiency**

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New Kinetis MCUs - SFPU Features

ARM® Cortex™-M4 MCUs

- ✓ Provides conversions between
  - ✓ fixed-point and floating-point data formats
  - ✓ floating-point constant instructions.
- ✓ Provides floating-point computation functionality that is compliant with the *ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic*.
- ✓ Sixteen 64-bit doubleword registers, D0-D15.
- ✓ Thirty-two 32-bit single-word registers, S0-S31.
- ✓ Fully supports Single-precision
  - ✓ *Add*
  - ✓ *Subtract*
  - ✓ *Multiply*
  - ✓ *Divide*
  - ✓ *Multiply and accumulate*
  - ✓ *Square root operations.*

K10 Family Summary — yy = package designator noted in the "Packages" column

Part Numbers	CPU Frequency (MHz)	Memory: Flash (KB)	Memory: FlexMemory (KB) EEPROM/DataFlash	Memory: SRAM (KB)	Memory: Cache (KB)	Feature Options: SFPU	MPU	SDHC	NFC	EBI	DAC	PGA	5V Tolerant I/O	Packages: 32QFN (5x5 mm)	48QFN (7 x7 mm)	48LQFP (7x7 mm)	64QFN (9x9 mm)	64LQFP (10x10 mm)	80LQFP (12x12 mm)	81BGA (10x10 mm)	100LQFP (14x14 mm)	104BGA (10x10 mm)	144LQFP (20x20 mm)	144BGA (13x13 mm)
MK10N32Vyy50	50	32	–	8										FM	FT	LF	FX	LH	LK	CB				
MK10N64Vyy50	50	64	–	16										FM	FT	LF	FX	LH	LK	CB				
MK10X32Vyy50	50	32	2/32	8										FM	FT	LF	FX	LH	LK	CB				
MK10X64Vyy50	50	64	2/32	16										FM	FT	LF	FX	LH	LK	CB				
MK10X128Vyy50	50	128	2/32	32						√	√	√	√				FX	LH	LK	CB	LL	ML		
MK10X128Vyy72	72	128	2/32	32						√	√	√	√				FX	LH	LK	CB	LL	ML		
MK10X256Vyy72	72	256	2/32	64						√	√	√	√						LK	CB	LL	ML		
MK10X128Vyy100	100	128	4/128	32			√	√		√	√	√	√										LQ	MD
MK10X256Vyy100	100	256	4/256	64			√	√		√	√	√	√										LQ	MD
MK10N512Vyy100	100	512	–	128			√	√		√	√	√	√						LK	CB	LL	ML	LQ	MD
MK10X512Vyy120	120	512	16/512	128	16	√	√	√	√	√	√	√	√										LQ	MD
MK10X512Vyy150	150	512	16/512	128	16	√	√	√	√	√	√	√	√										LQ	MD
MK10N1M0Vyy120	120	1024	–	128	16	√	√	√	√	√	√	√	√										LQ	MD
MK10N1M0Vyy150	150	1024	–	128	16	√	√	√	√	√	√	√	√										LQ	MD

>= 120MHz

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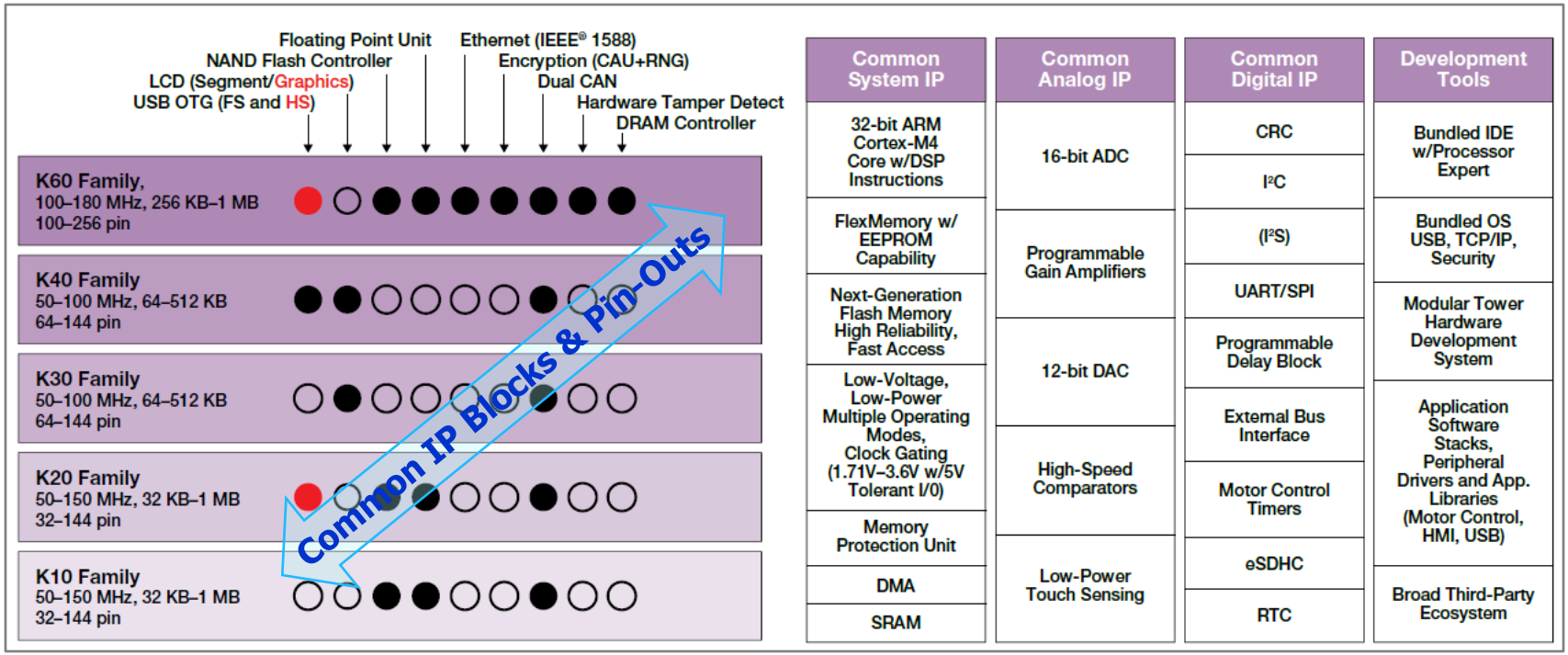
New Kinetis MCUs

More than 200 *NEW* Parts 7 scalable Family



32-bit Kinetis MCUs represent the most scalable portfolio of ARM® Cortex™-M4 MCUs in the industry. The *first phase* of the portfolio consists of five MCU families with over 200 pin-, peripheral- and software compatible devices with outstanding performance, memory and feature scalability. Enabled by innovative 90nm Thin Film Storage Flash with unique FlexMemory (configurable *embedded EEPROM*). Kinetis features the latest low-power innovations and high performance, high precision mixed-signal capability. Kinetis MCUs are supported by a market-leading enablement bundle from Freescale and ARM 3rd party ecosystem partners.

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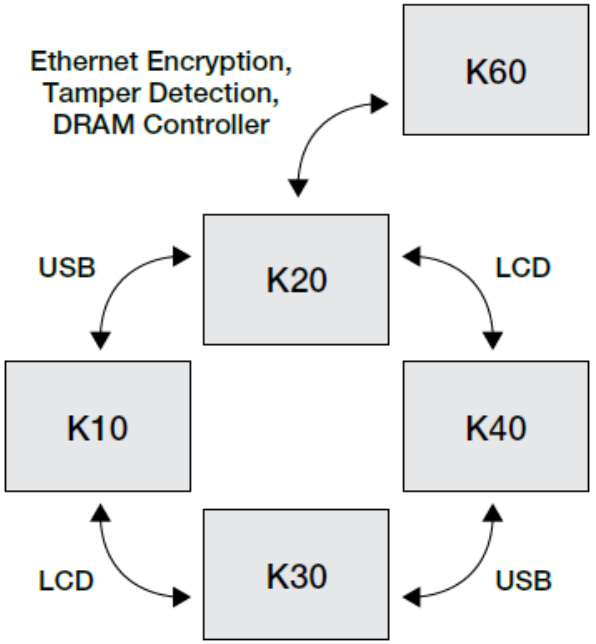
New Kinetis MCUs - Compatibility

ARM® Cortex™-M4 MCUs

To simplify your application's hardware and software design, all the Kinetis microcontroller families have unprecedented compatibility and scalability.

Kinetis Family	Differentiating Peripherals
K10	Baseline
K20	Baseline + USB
K30	Baseline + LCD
K40	Baseline + USB + LCD
K60	Baseline + USB + Ethernet + Encryption + Tamper Detect + DRAM Controller



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Kinetis MCUs

ARM® Cortex™-M4(F)
More than 200 NEW
Parts 7 scalable Family

Common **System IP**	Common **Analog IP**	Common **Digital IP**
32-bit ARM Cortex-M4 Core w/ DSP Instructions	16-bit ADCs	CRC
Next Generation Flash Memory High Reliability, Fast Access	Programmable Gain Amplifiers	I^2C
FlexMemory w/ EEPROM capability	12-bit DACs	SAI (I^2S)
SRAM		UARTs/SPIs
Memory Protection Unit	High-speed Comparators	Programmable Delay Block
eDMA		External Bus Interface
Low Voltage, Low Power Multiple Operating Modes, Clock Gating (1.71V-3.6V , optional with 5V tolerant I/O)	Low-power Touch Sensing	Motor Control Timers, PIT, LPT
-40°C to 105°C		eSDHC
		RTC

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Kinetis MCUs

Baseline

Common System IP	Common Analog IP	Common Digital IP
32-bit ARM Cortex-M4 Core w/ DSP Instructions	16-bit ADCs	CRC
		I^2C
Next Generation Flash Memory High Reliability, Fast Access	Programmable Gain Amplifiers	SAI (I^2S)
		UARTs/SPIs
FlexMemory w/ EEPROM capability	12-bit DACs	Programmable Delay Block
SRAM		External Bus Interface
Memory Protection Unit	High-speed Comparators	Motor Control Timers, PIT, LPT
eDMA		eSDHC
Low Voltage, Low Power Multiple Operating Modes, Clock Gating (1.71V-3.6V , optional with 5V tolerant I/O)	Low-power Touch Sensing	RTC
-40°C to 105°C		

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Kinetis MCUs

ARM® Cortex™-M4(F)
More than 200 NEW
Parts 7 scalable Family

	USB OTG (FS & HS)	Dual CAN *	Ethernet (IEEE 1588)	Encryption (CAU+RNG)	LCD (Segment/Graphics)	NAND Flash Controller	Floating Point Unit **	Hardware Tamper Detect	DRAM Controller ***
K60 256KB-1MB, 100-256pin	●	●	●	●		●	●	●	●
K40 64-512KB, 64-144pin	●	●			●				
K30 64-512KB, 64-144pin		●			●				
K20 32KB-1MB, 32-144pin	●	●				●	●		
K10 32KB-1MB, 32-144pin		●				●	●		

Common System IP	Common Analog IP	Common Digital IP
32-bit ARM Cortex-M4 Core w/ DSP Instructions	16-bit ADCs	CRC
Next Generation Flash Memory High Reliability, Fast Access	Programmable Gain Amplifiers	I^2C
FlexMemory w/ EEPROM capability	12-bit DACs	SAI (I^2S)
SRAM		UARTs/SPIs
Memory Protection Unit	High-speed Comparators	Programmable Delay Block
eDMA		External Bus Interface
Low Voltage, Low Power Multiple Operating Modes, Clock Gating (1.71V-3.6V , optional with 5V tolerant I/O)	Low-power Touch Sensing	Motor Control Timers, PIT, LPT
-40°C to 105°C		eSDHC
		RTC

*128k Flash and higher
[1 FlexCAN @ 64k Flash]
**120MHz & 150MHz only
***256 pin only

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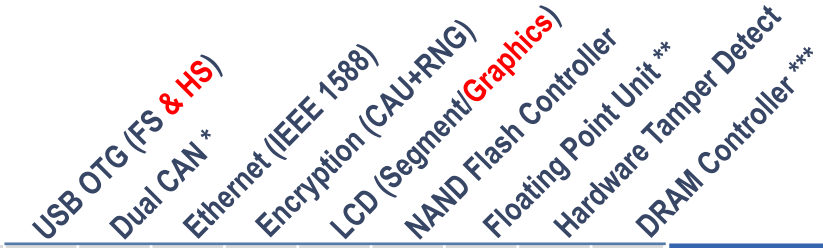
Kinetis MCUs

ARM® Cortex™-M4(F)
More than 200 NEW
Parts 7 scalable Family



	USB OTG (FS & HS)	Dual CAN *	Ethernet (IEEE 1588)	Encryption (CAU+RNG)	LCD (Segment/Graphics)	NAND Flash Controller	Floating Point Unit **	Hardware Tamper Detect	DRAM Controller ***
K70 512KB-1MB, 196-256pin	●	●	●	●	●	●	●	●	●
K60 256KB-1MB, 100-256pin	●	●	●	●		●	●	●	●
K50 128-512KB, 64-144pin	●		●	●	●				
K40 64-512KB, 64-144pin	●	●			●				
K30 64-512KB, 64-144pin		●			●				
K20 32KB-1MB, 32-144pin	●	●				●	●		
K10 32KB-1MB, 32-144pin		●				●	●		

Common System IP	Common Analog IP	Common Digital IP
32-bit ARM Cortex-M4 Core w/ DSP Instructions	16-bit ADCs	CRC
Next Generation Flash Memory High Reliability, Fast Access	Programmable Gain Amplifiers	I^2C
FlexMemory w/ EEPROM capability	12-bit DACs	SAI (I^2S)
SRAM	High-speed Comparators	UARTs/SPIs
Memory Protection Unit	Low-power Touch Sensing	Programmable Delay Block
eDMA		External Bus Interface
Low Voltage, Low Power Multiple Operating Modes, Clock Gating (1.71V-3.6V , optional with 5V tolerant I/O)		Motor Control Timers, PIT, LPT
-40°C to 105°C		eSDHC
		RTC

*128k Flash and higher
[1 FlexCAN @ 64k Flash]
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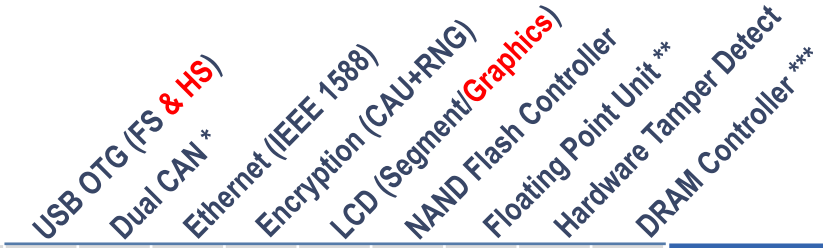
Kinetis MCUs

ARM® Cortex™-M4(F)
More than 200 NEW
Parts 7 scalable Family



	USB OTG (FS & HS)	Dual CAN *	Ethernet (IEEE 1588)	Encryption (CAU+RNG)	LCD (Segment/Graphics)	NAND Flash Controller	Floating Point Unit **	Hardware Tamper Detect	DRAM Controller ***
K70 512KB-1MB, 196-256pin	●	●	●	●	●	●	●	●	●
K60 256KB-1MB, 100-256pin	●	●	●	●		●	●	●	●
K50 128-512KB, 64-144pin	●		●	●	●				
K40 64-512KB, 64-144pin	●	●			●				
K30 64-512KB, 64-144pin		●			●				
K20 32KB-1MB, 32-144pin	●	●				●	●		
K10 32KB-1MB, 32-144pin		●				●	●		

Common System IP	Common Analog IP	Common Digital IP	Development
32-bit ARM Cortex-M4 Core w/ DSP Instructions	16-bit ADCs	CRC	Bundled IDE w/ Processor Expert
Next Generation Flash Memory High Reliability, Fast Access	Programmable Gain Amplifiers	I²C	Bundled OS USB, TCP/IP, Security
FlexMemory w/ EEPROM capability	12-bit DACs	SAI (I²S)	Modular Tower H/ware Development System
SRAM	High-speed Comparators	UARTs/SPIs	Application Software Stacks, Peripheral Drivers & App. Libraries (Motor Control, HMI, USB)
Memory Protection Unit	Low-power Touch Sensing	Programmable Delay Block	
eDMA		External Bus Interface	
Low Voltage, Low Power Multiple Operating Modes, Clock Gating (1.71V-3.6V , optional with 5V tolerant I/O)		Motor Control Timers, PIT, LPT	
-40°C to 105°C		eSDHC	Broad 3rd party ecosystem
		RTC	

*128k Flash and higher
[1 FlexCAN @ 64k Flash]
**120MHz & 150MHz only
***256 pin only

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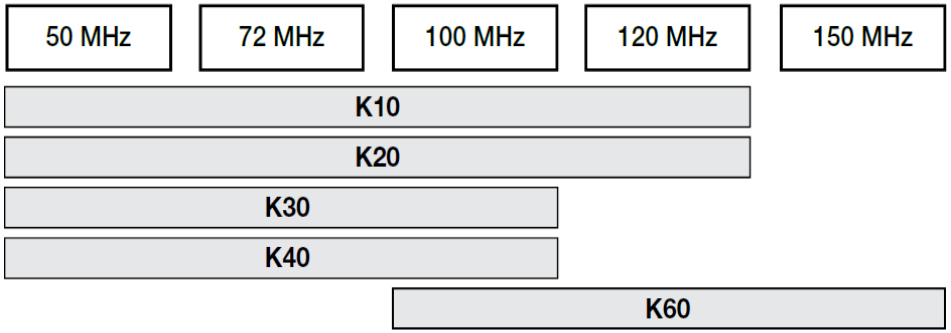
New Kinetis MCUs - Compatibility

ARM® Cortex™-M4 MCUs

To simplify your application's hardware and software design, all the Kinetis microcontroller families have unprecedented compatibility and scalability.



Operating Parameters	
Voltage Range (VDD)	1.71 to 3.6 V
Temperature Range (TA)	-40 to 105 C
Maximum CPU Frequency Tiers (Max. CPUCLK)	*50 MHz*
	72 MHz
	100 MHz
	120 MHz
	150 MHz

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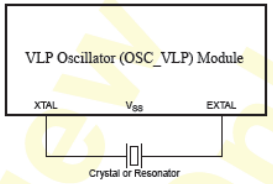
New Kinetis MCUs - Oscillator (OSC) Options

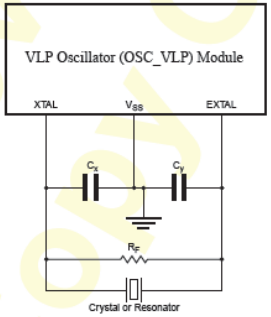
ARM® Cortex™-M4 MCUs

- ✓ Automatic Gain Control (AGC) to *optimize power consumption* in medium and high frequency ranges using low–power mode
- ✓ High gain option in all frequency ranges
- ✓ Voltage and frequency filtering to guarantee clock frequency and stability



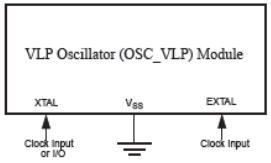
Configuration for crystal/resonator:

- ✓ Low Frequency, Low Power



Configuration for crystal/resonator:

- ✓ Low Frequency, High Gain
- ✓ High Frequency, Low Power
- ✓ High Frequency, High Gain



Configuration for external clock

OSC Clock Sources	
External crystal oscillator or resonator	Low Range: 32 – 40 kHz
	Medium Range: 1 – 8 MHz
	High Range: 8 – 32 MHz
External square wave input clock	DC to 50 MHz

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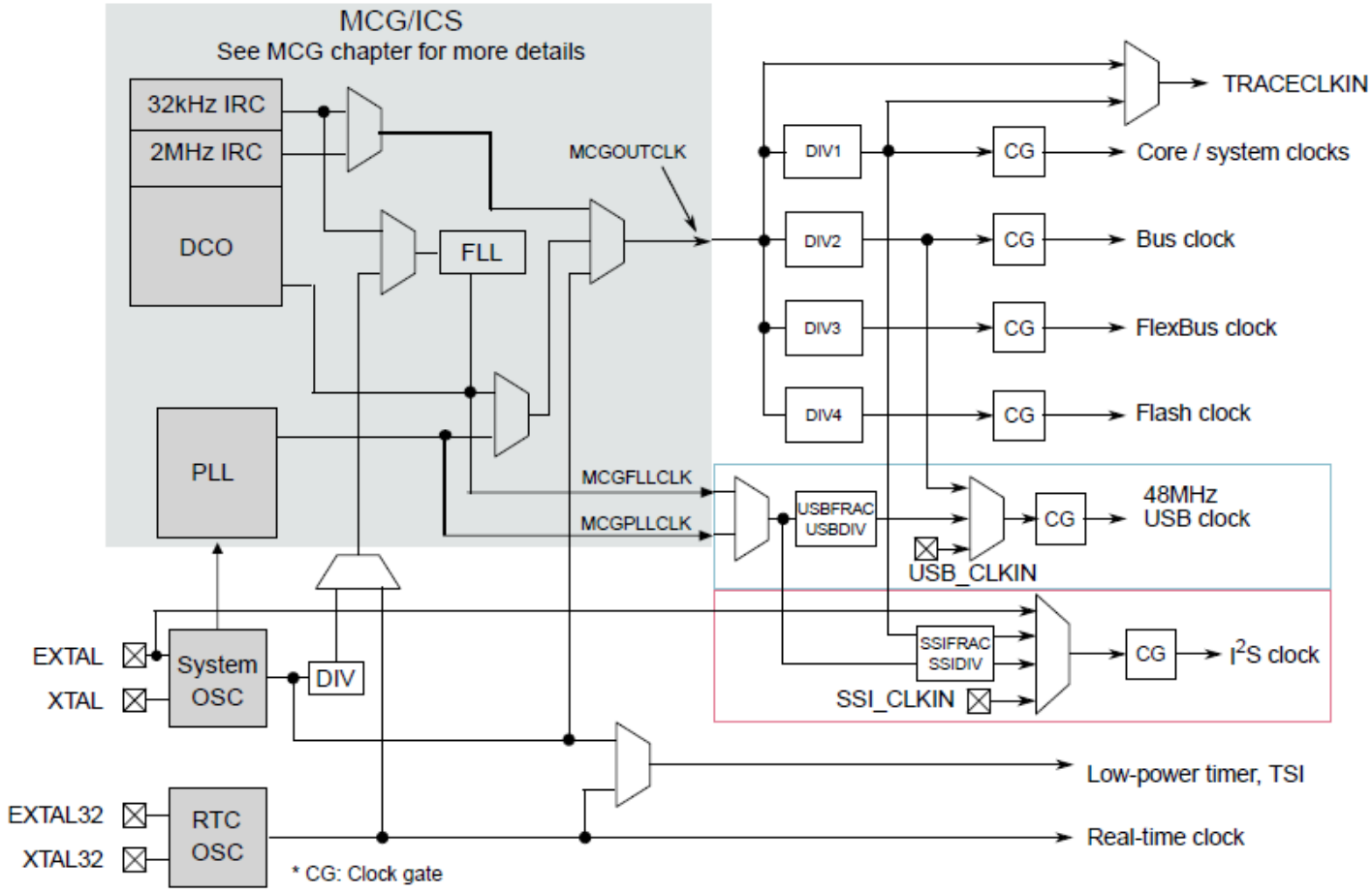
New Kinetis MCUs - Multiple Clock System (MCG)

ARM® Cortex™-M4 MCUs



Clocking Diagram

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New Kinetis MCUs - Multiple Clock System (MCG)

The Power Management Controller (PMC) generates a 1kHz clock (1kHz LPO) that is enabled in all modes of operation, including all low power modes.

This 1-kHz source is commonly referred to as LPO clock or 1-kHz LPO clock.

This clock feeds the following destinations:

- ✓ Watchdog
- ✓ External watchdog monitor (EWM)
- ✓ Low-Power timer
- ✓ Port Control digital clitch filters
- ✓ Reset glitch filter

Class B: IEC 60730 compliant by providing system robustness, diagnostic and self test mechanisms to ensure safe operation of hardware and software in application

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New Kinetis MCUs - Watchdog

ARM® Cortex™-M4 MCUs

- ✓ Independent clock source input and choice for different clock connections (independent from CPU/Bus clock)
- ✓ Unlock sequence for allowing updates to write-once WDOG Control/Configuration bits.
- ✓ All WDOG Control/Configuration bits are writeable once only, within 256 bus clock cycles of being unlocked.
  - ✓ Users need to always update these after unlocking, within 256 bus clock cycles. Failure to update resets the system.
- ✓ Programmable Timeout period, specified in terms of number of WDOG clock cycles.
- ✓ Window Refresh Option, programmable window
- ✓ Ability to test WDOG timer and reset, with flag indicating watchdog test. This test can be permanently disabled.
  - ✓ Quick Test – Small timeout value programmed for quick test.
  - ✓ Byte Test – Individual bytes of timer tested one at a time.

Software RESET
'SYSRESETREQ' bit in the NVIC can be set to force a software reset on the device.
This reset forces a system reset of all major components except for the debug module. A software reset causes SRSH[SW] bit to set.

Class B: IEC 60730 compliant by providing system robustness, diagnostic and self test mechanisms to ensure safe operation of hardware and software in application

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New Kinetis MCUs - External Watchdog Monitor (EWM)

ARM® Cortex™-M4 MCUs

- ✓ Independent 1kHz LPO clock source input (independent from CPU/Bus clock)
- ✓ Programmable Timeout period, specified in terms of number of EWM clock cycles
- ✓ Windowed Refresh Option
  - ✓ Provides robust check that program flow is faster than expected
  - ✓ Programmable window
  - ✓ Refresh outside window leads to EWM_OUT_b pin assertion
- ✓ Robust refresh mechanism

  Write values of 0xB4 and 0x2C to EWM Refresh Register within

  15 bus clock cycles of each other, to WDOG Refresh Register

For safety, a redundant watchdog system, External Watchdog Monitor (EWM), is designed to monitor external circuits, as well as the MCU software flow. This provides a back-up mechanism to the internal watchdog that resets the MCU's CPU and peripherals.

- ✓ One output pin, EWM_OUT pin, when asserted

  is used to reset or place the external circuit into safe mode
- ✓ One input pin, EWM_IN, allows an external circuit to control the EWM_OUT pin

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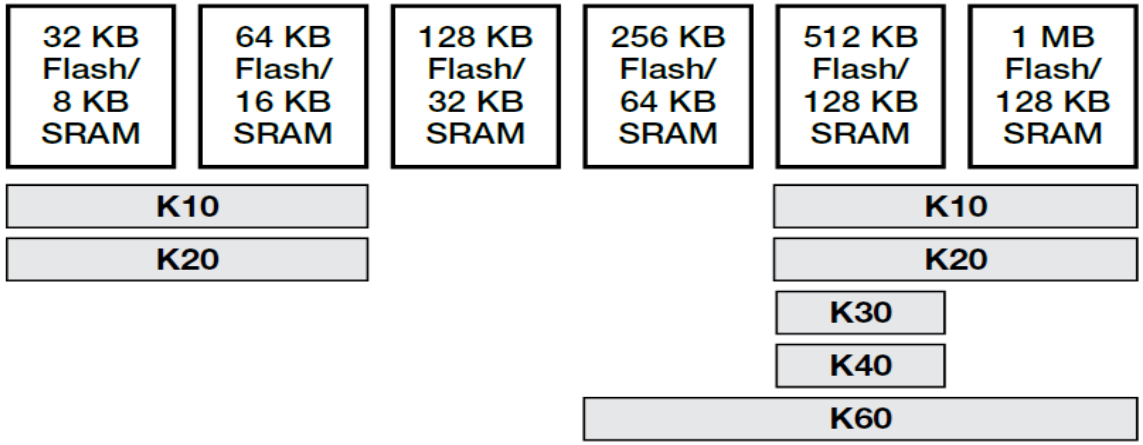
New Kinetis MCUs - Compatibility

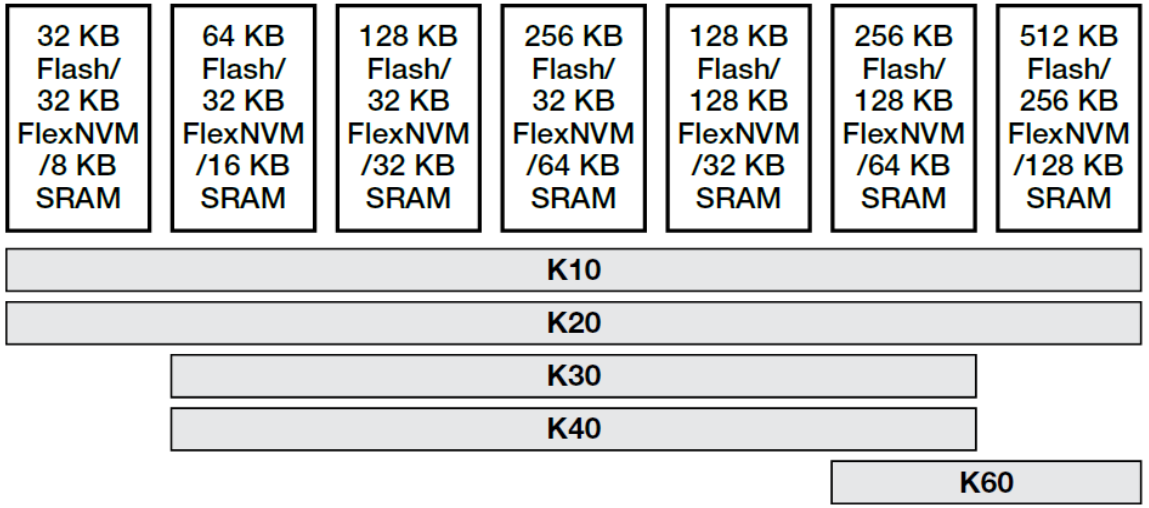
ARM® Cortex™-M4 MCUs

Kinetis Families WITHOUT FlexMemory



4:1 Flash:RAM

Kinetis Families WITH FlexMemory



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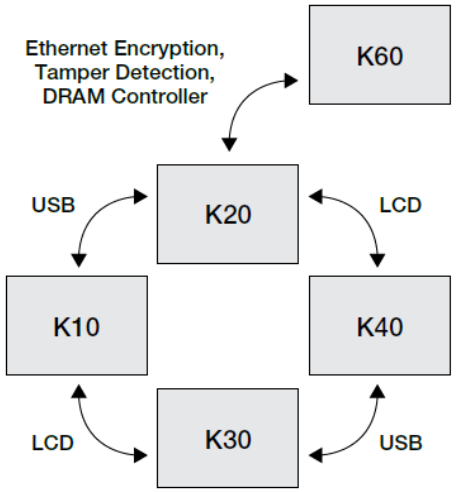
New Kinetis MCUs - Compatibility

ARM® Cortex™-M4 MCUs

Type	Body Size	Pitch	Families
32-pin QFN	5 x 5 mm	0.5 mm	K10, K20
48-pin QFN	7 x 7 mm	0.5 mm	K10, K20
48-pin LQFP	7 x 7 mm	0.5 mm	K10, K20
64-pin QFN	9 x 9 mm	0.5 mm	K10, K20, K30, K40
64-pin LQFP	10 x 10 mm	0.5 mm	K10, K20, K30, K40
80-pin LQFP	12 x 12 mm	0.5 mm	K10, K20, K30, K40
81-pin MAPBGA	8 x 8 mm	0.65 mm	K10, K20, K30, K40
100-pin LQFP	14 x 14 mm	0.5 mm	K10, K20, K30, K40, K60
121-pin MAPBGA	8 x 8 mm	0.65 mm	K10, K20, K30, K40, K60
144-pin LQFP	20 x 20 mm	0.5 mm	K10, K20, K30, K40, K60
144-pin MAPBGA	13 x 13 mm	1.0 mm	K10, K20, K30, K40, K60
196-pin MAPBGA	15 x 15 mm	1.0 mm	K60
256-pin MAPBGA	17 x 17 mm	1.0 mm	K60



QFN/LQFP Packages:

Optimized for 2 layer board designs

MAPBGA Packages:

Optimized for 4 layer board designs

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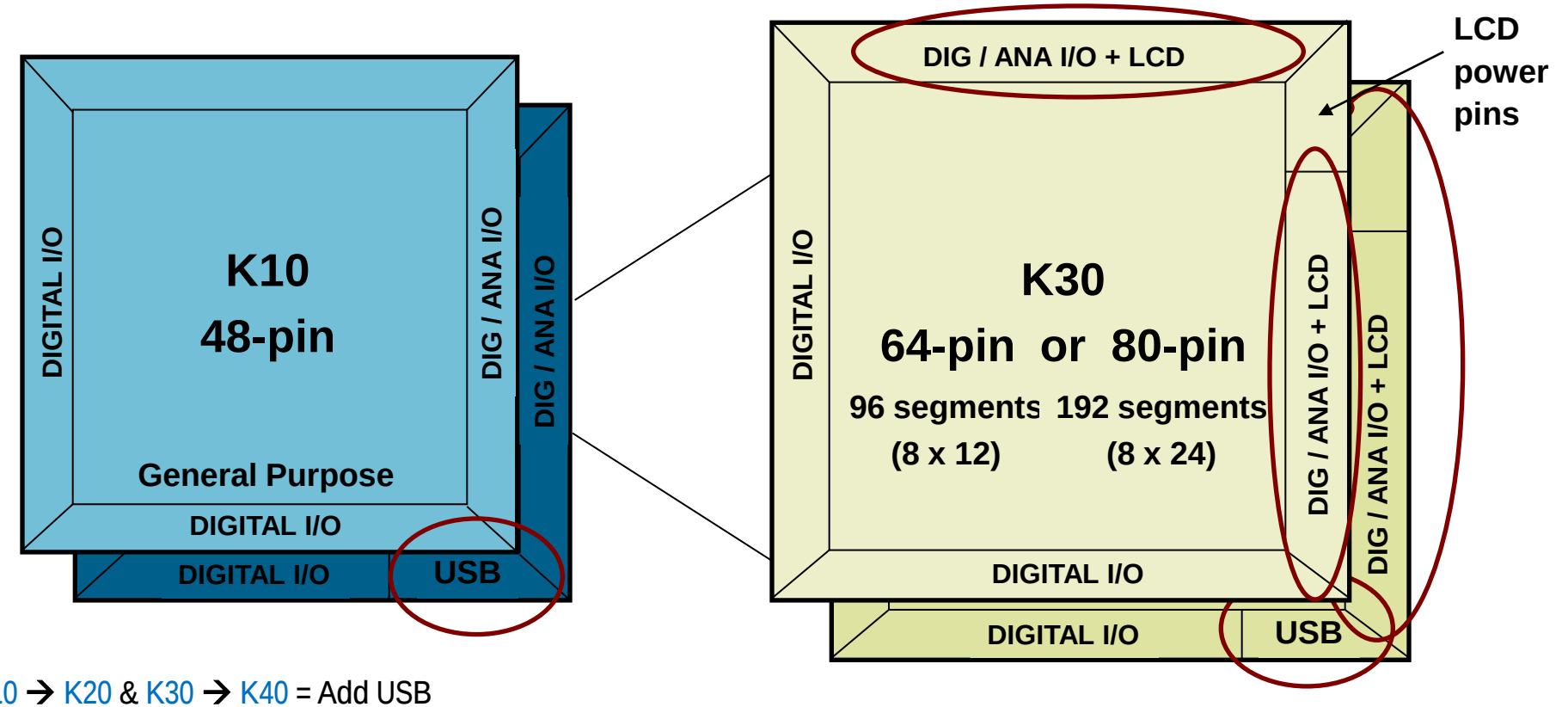
DIGITAL I/O = UART, SPI, I2C, CAN, TIMER, etc.
ANALOG I/O = OSC, ADC, CMP, etc.

New Kinetis MCUs - Compatibility



K10 → K20 & K30 → K40 = Add USB

- *The only difference will be 4 extra USB pins and 4 less digital I/O pins*

K10 → K30 & K20 → K40 = Add Segment LCD

- *Digital & Analog I/O signals maintain placement order*
- *Segment LCD signals are muxed with existing Digital & Analog I/O signals*
- *Most Digital I/O signals muxed with Segment LCD signals become available on added pins by larger package*

K20 → K60 = Add Ethernet

- *All Ethernet signals are muxed with existing Digital & Analog I/O signals*

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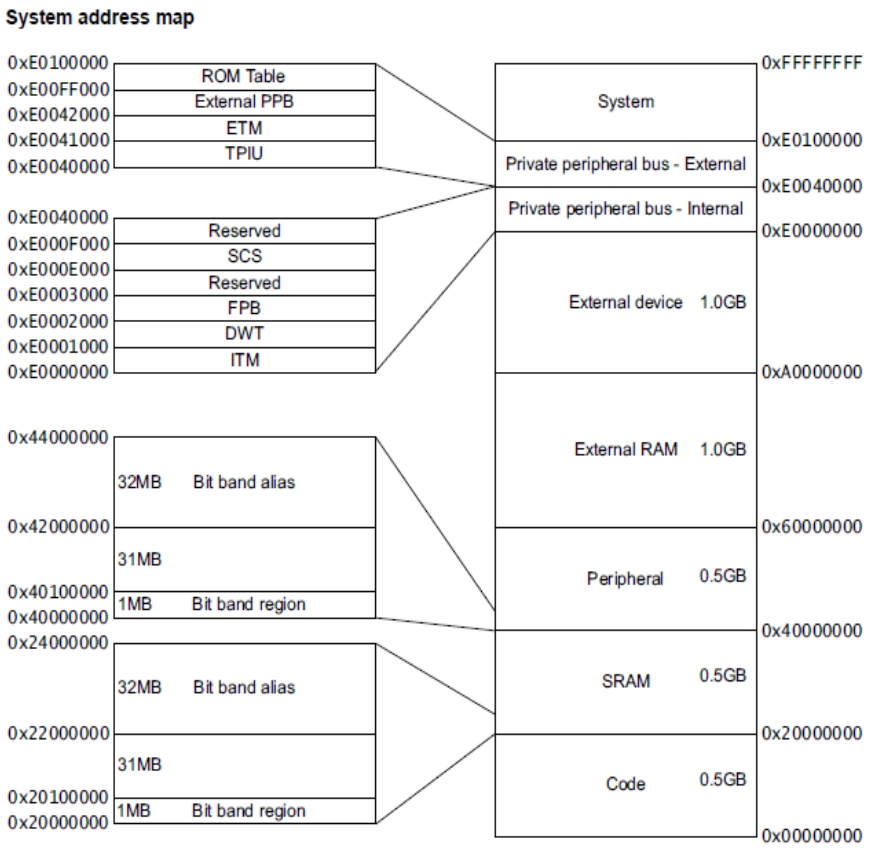
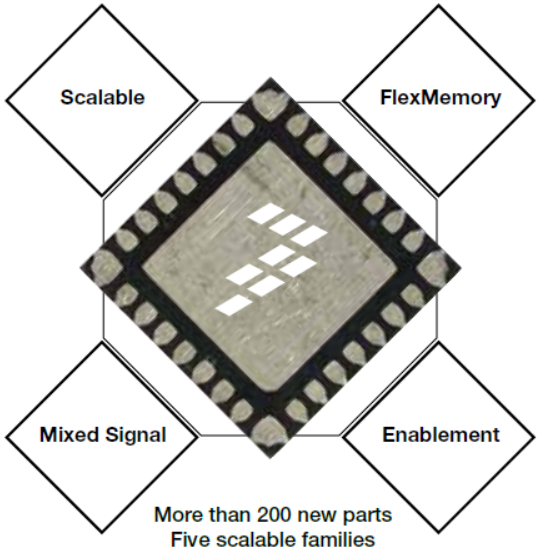
New Kinetis MCUs - Memory / Compatibility

ARM® Cortex™-M4 MCUs Memory Map





For more Details: Cortex®-M4 Technical Reference Manual (Revision r0p1)

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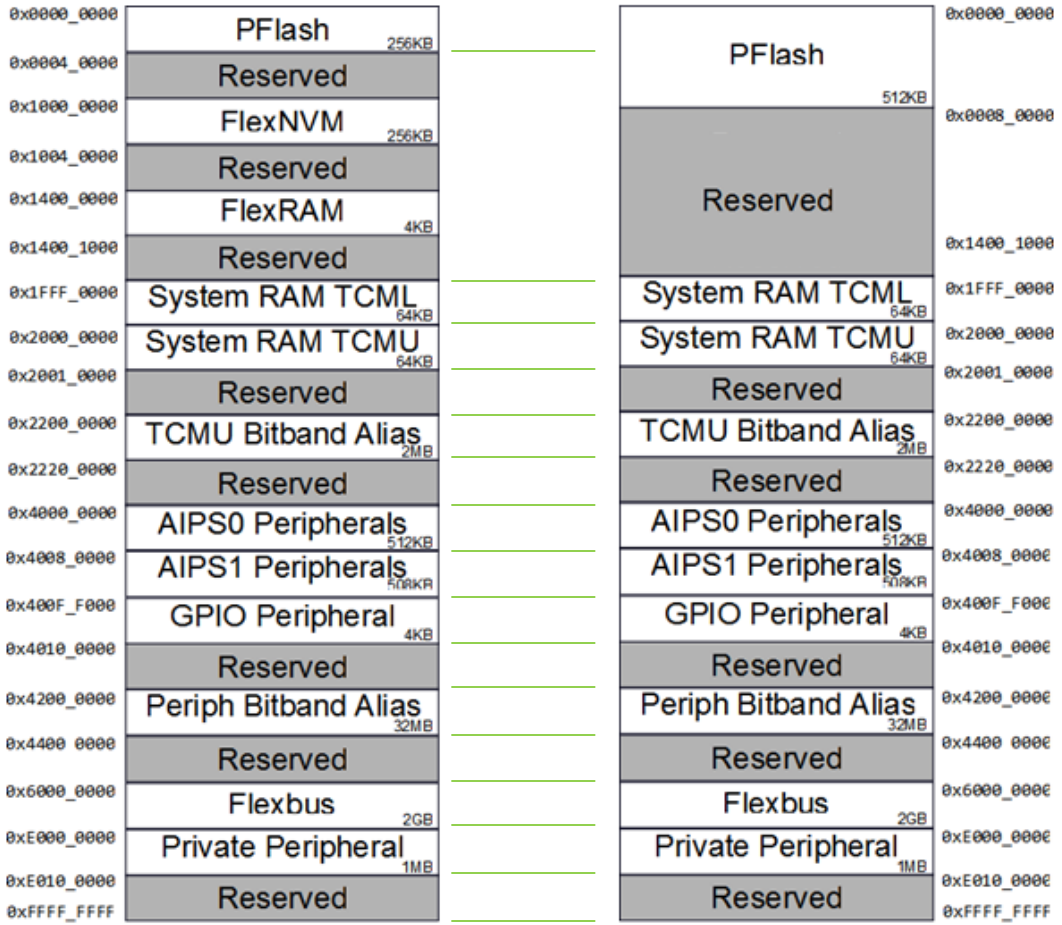
New Kinetis MCUs - Memory / Compatibility

ARM® Cortex™-M4 MCUs

Independent Flash banks enable concurrent code execution and firmware Updates

The program flash blocks support a swap feature in which the starting address can be swapped.

(devices with program flash only have 2 contiguous blocks of program flash in the memory map)



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New Kinetis MCUs - Flash Programming

ARM® Cortex™-M4 MCUs

There are several options availabe for programming

the on-chip flash for Pioneer family devices:

✓ JTAG/cJTAG: *Debugger interfaces with programming capability*

✓ EzPort: *SPI flash style programming interface*

Updated version of the module available on Kirin family parts

✓ Software : *Resident flash programming routines useful for firmware updates in the field*

EzPort Feature: Serial interface that is compatible with a subset of the SPI format.

- Able to read, erase and program flash memory
- Supports section program command for most efficient programming

Able to reset the micro-controller, allowing it to boot from the flash memory after the memory has been configured

- EzPort can be made available on the JTAG header (10-pin or 20-pin)
- EzPort can program the flash faster than JTAG
  - *Using EzPort on JTAG header allows for faster programming option without needing an additional header*
  - *Will be supported by CodeWarrior tool chain*
- EzPort force disable option bit in flash option register
  - *User programmable bit that can disable entry into EzPort mode*
  - *Prevents accidental entry into EzPort mode*
  - *Extra system security (prevents EzPort from being used as a security exploit)*

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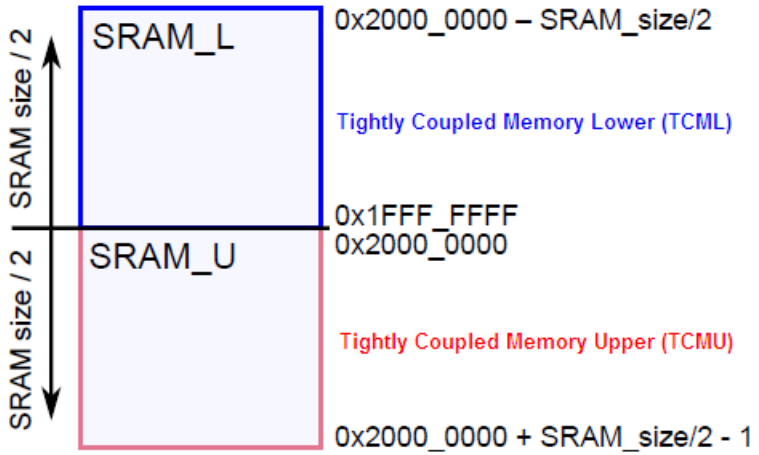
New Kinetis MCUs - SRAM

SRAM performance for core accesses:

- ✓ Instruction fetch from TCML has zero wait states
- ✓ Instruction fetch from TCMU has one wait state
- ✓ Data fetch from TCML and TCMU have zero wait states

Access to invalid memory regions will cause a transfer access error exception



The on-chip SRAM is implemented with TCML:TCMU ranges forming a contiguous block of memory.

SRAM retained in low Power modes

- ✓ The SRAM is retained down to VLLS3 mode
- ✓ In VLLS2 the 4kB region of SRAM_U [0x2000_0000 to 0x2000_0FFF] is powered
- ✓ In VLLS1 no SRAM is retained. However, the 32byte regsiter file is available

The following simultaneous accesses can be made to TCML and TCMU SRAM arrays:

- ✓ Core instruction (TCML) and core data (TCMU)
- ✓ Core instruction (TCML) and non-core master (TCMU)
- ✓ Core data (TCMU) and non-core master (TCML)
- ✓ Two non-core masters cannot access the same SRAM array simultaneously because of XBS (Crossbar Switch) arbitration

SRAM SIZE OPTIONS (KB)	TCML (KB)	TCMU (KB)
128	64	64
96	32	64
64	32	32
32	16	16

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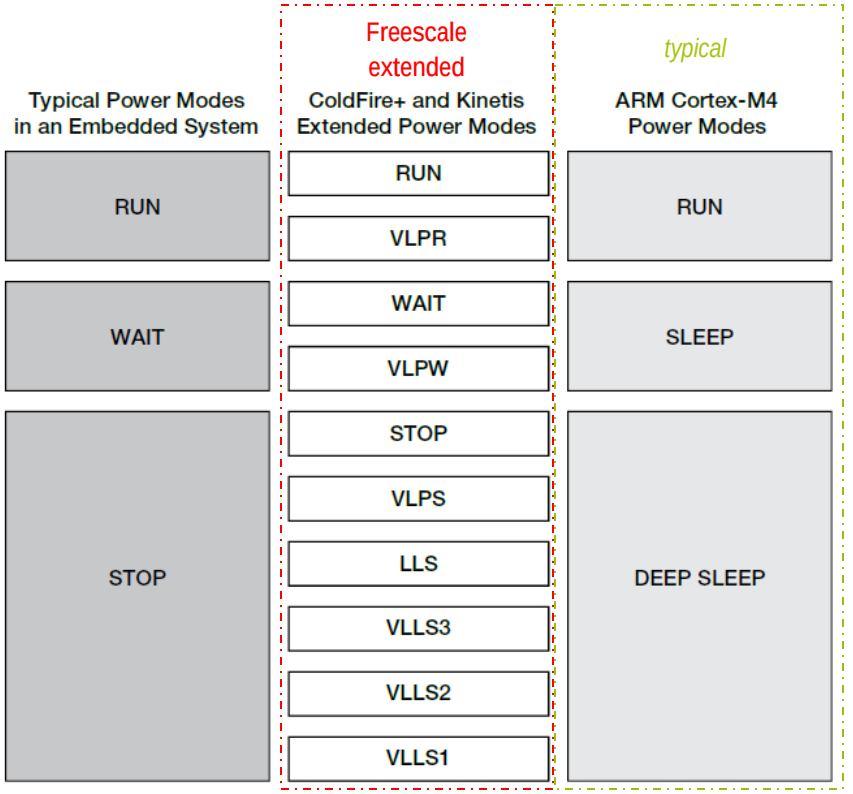
New Kinetis MCUs - Low Power Modes

ARM® Cortex™-M4 MCUs

Low Power Modes:

10 modes of operation are supported to allow the user to optimize power consumption for the level of functionality needed.

Key Features	Customer Benefits
Nano-amp current consumption with RAM retention	Extended battery life
Wake-up time as fast as 4 uS	Minimize average power consumption in frequent power mode change applications
Multiple power modes	Full flexibility for functionality vs. power consumption
200 uA/MHz normal run mode	Device can be active with minimal power consumption



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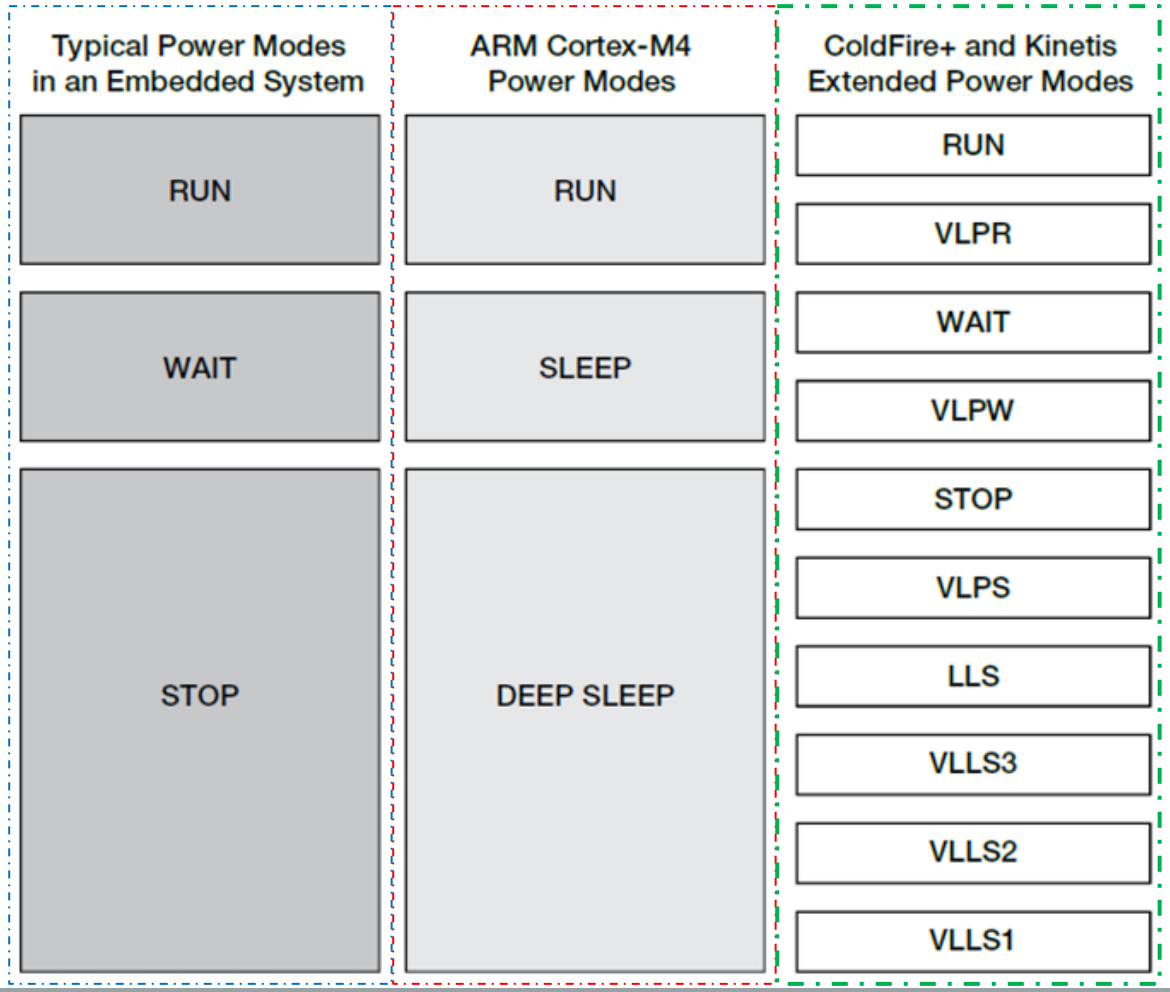
New Kinetis MCUs - Low Power Modes

ARM® Cortex™-M4 MCUs



	Typical Recovery Time:	IDD: Starting @ <200uA/MHz
VLPW	4us	
STOP	4us	
VLPS	4us	
LLS	4us	1.2uA - 7uA
VLLS3	35us	1uA - 5uA
VLLS2	35us	750nA - 2uA
VLLS1	100us *+ EE restore*	500nA – 1.5uA

Values subject to change

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New Kinetis MCUs - Low Power Modes

ARM® Cortex™-M4 MCUs

Mode	Definition
Run	MCU can be run at full speed.
Wait	Allows peripherals to function, while CPU goes to sleep reducing power consumption.
VLP Run	CPU and peripheral clock maximum frequency is restricted. CPU/Platform clock is restricted to 2MHz. Flash access is restricted to 1MHz. LVD is off.
VLP Wait	Similar to VLP Run, with CPU in sleep to further reduce power.
Stop	MCU is in static state. Lowest power mode that retains all registers while maintaining LVD protection.
VLP Stop	MCU is in static state with LVD operation off. Lowest power mode with ADC, LPT, RTC, LCD, HSCMP, DAC, and pin interrupts functional.
LL Stop	MCU is in low leakage state retention power mode. LLWU controls wakeup sources including LPT, RTC, LCD, HSCMP, DAC and select pin interrupts.
VLL Stop 3	Powering down most internal logic. All system RAM contents are retained and I/O states held. LLWU controls wakeup sources (up to 16 GPIOs, LPT, RTC, LCD, HSCMP, and DAC)
VLL Stop 2	Similar to VLL Stop 3, partial system RAM retention. FlexRAM contents can optionally be retained.
VLL Stop 1	Similar to VLL Stop 3, with only 32 byte register file retention.

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New Kinetis MCUs - Low Power Modes

Modules	STOP	VLPR	VLPW	VLPS	LLS	VLLSx
Regulator	ON	low power	low power	low power	low power	low power
LVD	ON	disabled	disabled	disabled	disabled	disabled
1kHz LPO	ON	ON	ON	ON	ON	ON
System oscillator (OSC)	ERCLK optional	ERCLK max of 4MHz crystal	ERCLK max of 4MHz crystal	ERCLK max of 4MHz crystal	limited to low range/low power	limited to low range/low power
MCG	static - IRCLK optional; PLL optionally on but gated	2 MHz IRC	2 MHz IRC	static - no clock output	static - no clock output	OFF
Core Clock	OFF	2 MHz max	OFF	OFF	OFF	OFF
System Clock	OFF	2 MHz max	2MHz max	OFF	OFF	OFF
Bus Clock	OFF	2 MHz max	2 MHz max	OFF	OFF	OFF
Flash	powered	1 MHz max access - no pgm	low power	low power	OFF	OFF
Portion of SRAM_U[1]	powered	powered	powered	powered	powered	powered in VLLS3,2
Remaining SRAM_U and all of SRAM_L	powered	powered	powered	powered	powered	powered in VLLS3
FlexMemory[2]	powered	powered[3]	powered	powered	powered	powered in VLLS3, optionally powered in VLLS2
Register File	powered	powered	powered	powered	powered	powered
DMA	static	FF	FF	static	static	OFF
UART[4]	static, wakeup on edge	125 kbps	125 kbps	static, wakeup on edge	static	OFF
SPI[5]	static	1 Mbps	1 Mbps	static	static	OFF

FF = Fully Functional

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New Kinetis MCUs - Low Power Modes

Modules	STOP	VLPR	VLPW	VLPS	LLS	VLLSx
I^2C[6]	static, address match wakeup	100 kbps	100 kbps	static, address match wakeup	static	OFF
CAN[7]	wakeup	FF	FF	wakeup	static	OFF
I^2S	static	FF	FF	static	static	OFF
TSI	wakeup	FF	FF	wakeup	wakeup[8]	wakeup[8]
FTM	static	FF	FF	static	static	OFF
PIT	static	FF	FF	static	static	OFF
PDB	static	FF	FF	static	static	OFF
LPT	FF	FF	FF	FF	FF	FF
Watchdog	FF	FF	FF	FF	static	OFF
EWM	static	FF	static	static	static	OFF
16-bit ADC	ADC internal clock only	FF	FF	ADC internal clock only	static	OFF
CMP[9]	HS or LS compare	FF	FF	HS or LS compare	LS compare	LS compare
6-bit DAC	static	FF	FF	static	static	static
VREF	FF	FF	FF	FF	static	OFF
12-bit DAC	static	FF	FF	static	static	static
USB FS/LS	static	static	static	static	static	OFF
USB DCD	static	FF	FF	static	static	OFF
USB Voltage Regulator	optional	optional	optional	optional	optional	optional

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New Kinetis MCUs - Low Power Modes

Modules	STOP	VLPR	VLPW	VLPS	LLS	VLLSx
Ethernet	wakeup	static	static	static	static	OFF
RTC - 32kHz OSC	FF	FF	FF	FF	FF	FF
EzPort	disabled	disabled	disabled	disabled	disabled	disabled
SDHC	wakeup	FF	FF	wakeup	static	OFF
GPIO	wakeup	FF	FF	wakeup	static, pins latched	OFF, pins latched
FlexBus	static	FF	FF	static	static	OFF
CRC	static	FF	FF	static	static	OFF
RNGB	static	FF	static	static	static	OFF
CMT	static	FF	FF	static	static	OFF
NVIC	static	FF	FF	static	static	OFF
Mode Controller	FF	FF	FF	FF	FF	FF
LLWU[10]	static	static	static	static	FF	FF

1. The 4KB portion of SRAM_U from 0x2000_0000 to 0x2000_0FFF block is the region of RAM left powered on in low power mode VLLS2.
2. FlexMemory is always powered in VLLS3. When used as FlexNVM is powered in VLLS2. When not used as FlexNVM, user can optionally enable powering FlexRAM in VLLS2.
3. FlexMemory enabled as FlexNVM is not writable in VLPR and writes are ignored. Read accesses to FlexNVM while in VLPR are allowed. There are no access restrictions for FlexMemory configured as FlexRAM.
4. UART clocked from 2 MHz in VLP supports 125kbps.
5. SPI clocked from 2 MHz in VLP supports 1Mbps.
6. I2C clocked from 2 MHz in VLP supports 100kbps.
7. CAN clocked from 2 MHz in VLP supports 256kbps.
8. TSI wakeup from LLS and VLLSx modes is limited to a single selectable pin.
9. CMP in stop or VLPS supports high speed or low speed external pin to pin or external pin to DAC compares. CMP in LLS or VLLSx only supports low speed external pin to pin or external pin to DAC compares. Windowed, sampled & filtered modes of operation are not available while in stop, VLPS, LLS, or VLLSx modes.
10. Using the LLWU module, the external pins available for this chip do not require the associated peripheral function to be enabled. It only requires the function controlling the pin (GPIO or peripheral) to be configured as an input to allow a transition to occur to the LLWU.

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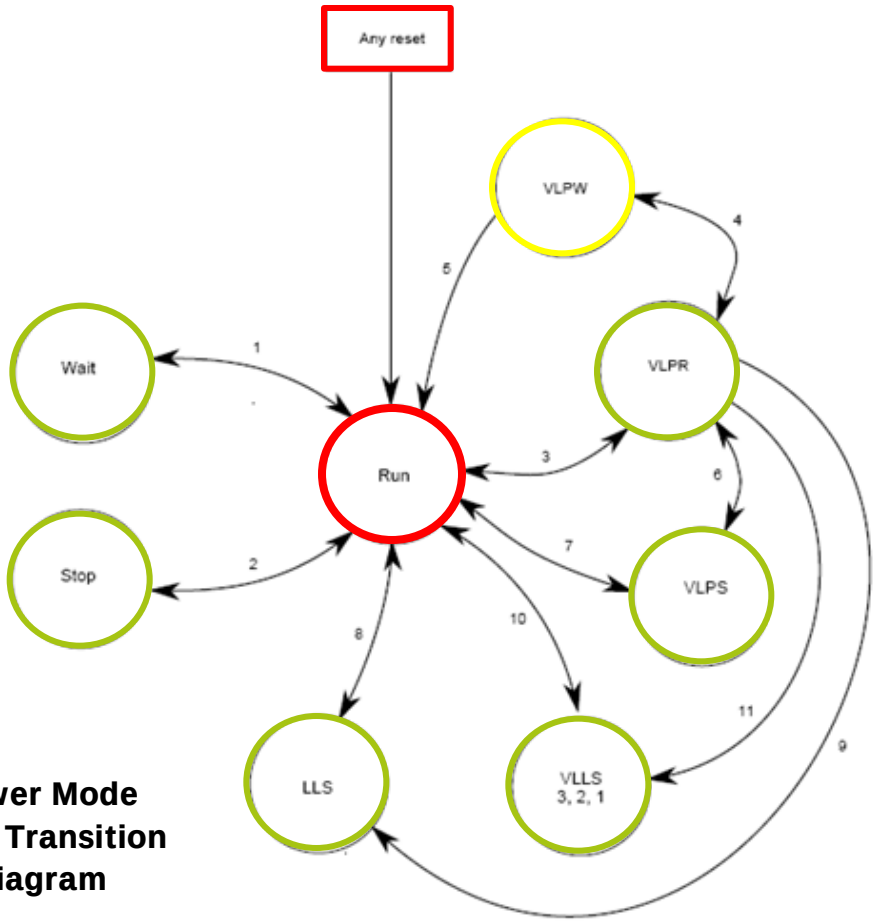
New Kinetis MCUs - Low Power Modes

ARM® Cortex™-M4 MCUs



Power Mode State Transition Diagram

Additional enhancements:

- ✓ Clock gating
- ✓ Power gating
- ✓ Direct Mode Transition

Typical Power Modes in an Embedded System	Freescale ColdFire+ and Kinetis Extended Power Modes	typical ARM Cortex-M4 Power Modes
RUN	RUN	RUN
	VLPR	
WAIT	WAIT	SLEEP
	VLPW	
STOP	STOP	DEEP SLEEP
	VLPS	
	LLS	
	VLLS3	
	VLLS2	
	VLLS1	

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New Kinetis MCUs - LLWU Features

Low-Leakage Wake-up Unit

- ✓ Supports up to 16 external input pins and up to 8 internal modules with individual enable bits for wakeup sources. Input sources may be external pins or from internal peripherals capable of running in LLS or VLLS. See Wake-up Sources for wakeup input sources for Pioneer Series devices.
- ✓ Each external pin wakeup input is programmable as falling edge, rising edge, or any edge
- ✓ An optional 3 LPO cycle digital filter provided to qualify an external pin detect.
  With glitch filter enabled, external pin wakeup input is programmable to falling or rising edge only.
- ✓ Each internal module wakeup input uses the modules interrupt flag qualified with interrupt enable as wakeup source
- ✓ Wakeup inputs are activated if enabled once MCU enters Low Leakage Stop (LLS) or Very Low Leakage Stop (VLLS) modes
- ✓ Exit via a CPU interrupt request when MCU is in LLS unless via RESET pin
- ✓ Exit via reset flow when MCU is in VLLS. I/O states remain in held state until wakeup has been acknowledged.
- ✓ Supports debug entry request immediately upon exit from LLS and VLLS modes

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New Kinetis MCUs - LLWU Wakeup Sources

Low-Leakage Wake-up Unit

LLWU Inputs Example (K60)

Wakeup pin	Source		Wakeup pin	Source
LLWU_P0	PTE1/SCI1_RX/I2C1_SCL		LLWU_P12	PTD0/DSPI0_PCS0/$\overline{\text{SCI2\_RTS}}$
LLWU_P1	PTE2/DSPI1_SCK/SDHC0_DCLK		LLWU_P13	PTD2/SCI2_RX
LLWU_P2	PTE4/DSPI1_PCS0/SDHC0_D3		LLWU_P14	PTD4/$\overline{\text{SCI0\_RTS}}$/FTM0_CH4/EWM_IN
LLWU_P3	PTA4/FTM0_CH1/$\overline{\text{NMI}}$		LLWU_P15	PTD6/SCI0_RX/FTM0_CH6/FTM0_FLT0
LLWU_P4	PTA13/CAN0_RX/FTM1_CH1 /FTM1_QD_PHB		LLWU_M0IF	LPT (see note 1)
LLWU_P5	PTB0/I2C0_SCL/FTM1_CH0/FTM1_QD_PHA		LLWU_M1IF	CMP0 (see note 1)
LLWU_P6	PTC1/$\overline{\text{SCI1\_RTS}}$/FTM0_CH0		LLWU_M2IF	CMP1 (see note 1)
LLWU_P7	PTC3/SCI1_RX/FTM0_CH2		LLWU_M3IF	CMP2 (see note 1)
LLWU_P8	PTC4/DSPI0_PCS0/FTM0_CH3		LLWU_M4IF	TSI (see note 1)
LLWU_P9	PTC5/DSPI0_SCK		LLWU_M5IF	RTC (see note 1)
LLWU_P10	PTC6/PDB0_EXTRG		LLWU_M6IF	Reserved
LLWU_P11	PTC11/SSI0_RXD		LLWU_M7IF	Error Detect - wake-up source unknown

The LLWU allows up to 16 external pins , the RESET pin, and up to seven internal peripherals to wake the MCU from LLS and VLLSx power modes.

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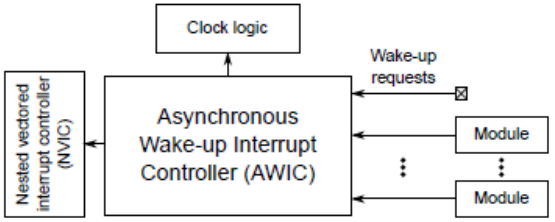
New Kinetis MCUs - AWIC

Asynchronous Wake-up Interrupt Controller

Wake-up source	Description
Reset	$\overline{\text{RESET}}$ pin
Low-voltage detect	Mode Controller
Low-voltage warning	Mode Controller
Pin interrupts	Port Control Module - Any enabled pin interrupt is capable of waking the system
ADCx	The ADC is functional when using internal clock source
CMPx	Since no system clocks are available, functionality is limited
I^2C	Address match wakeup
UART	Active edge on RXD
USB	Wakeup
LPT	
RTC	
Ethernet	Magic Packet wakeup
SDHC	Wakeup
TSI	
CAN	



AWIC Stop and VLPS Wake-up Sources

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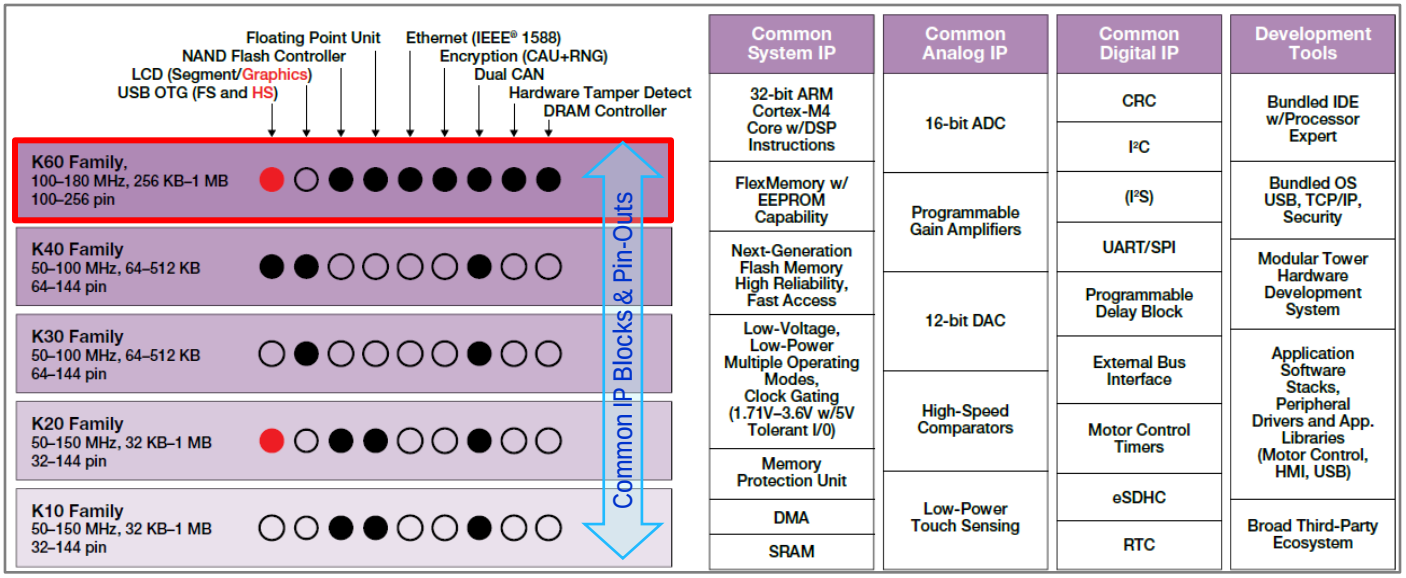
New Kinetis MCUs - Feature Overview

ARM® Cortex™-M4 MCUs

The K60 MCU family includes IEEE 1588 Ethernet, full- and high-speed USB 2.0 On-The-Go *with device charger detect capability*, hardware encryption and *tamper detection capabilities*. Devices start from 256 KB of flash in 100LQFP packages extending up to 1 MB in a 256MAPBGA package with a rich suite of analog, communication, timing and control peripherals. High memory density K60 family devices include an optional single precision floating point unit, NAND flash controller and DRAM controller.



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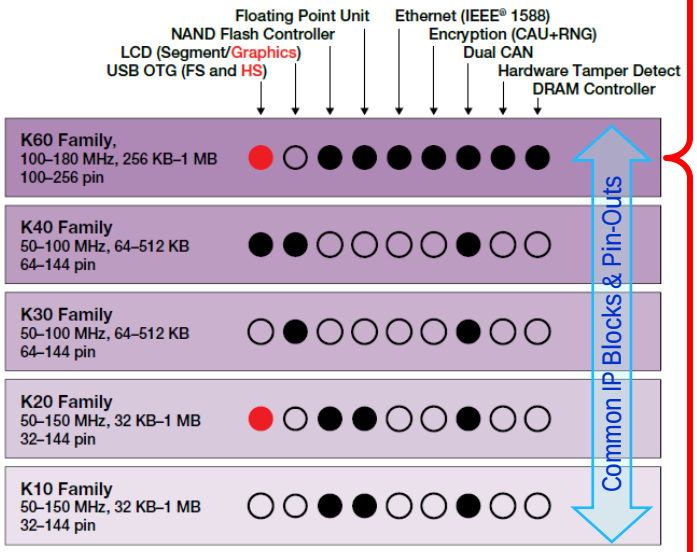
New Kinetis MCUs - Feature Overview

Note:

Features are Optional according to Family, Performance and Package - like SFFPU, Ethernet, LCD, and NAND- / DDR-CTRL



Core
ARM Cortex M4

- Debug Interfaces
- DSP
- Interrupt Controller
- Floating Point Unit

System

- Internal and External Watchdogs
- Memory Protection
- DMA
- Low-Leakage Wake-Up

Memories

- Program Flash
- RAM
- FlexMemory
- Cache
- Serial Programming Interface
- External Bus
- NAND Flash Controller
- DDR Controller

Clocks

- Phase-Locked Loop
- Frequency-Locked Loop
- Low/High-Frequency Oscillators
- Internal Reference Clocks

Security

- Cyclic Redundancy Check
- Random Number Generator
- Hardware Encryption
- Tamper Detect

Analog

- 16-bit ADC x4
- PGA x4
- Analog Comparator x3
- 6-bit DAC x3
- 12-bit DAC x2
- Voltage Reference

Timers

- Timers x4 (20-ch.)
- Carrier Modulator Transmitter
- Programmable Delay Block
- Periodic Interrupt Timers
- Low-Power Timer
- Independent Real-Time Clock
- IEEE 1588 Timers

Communication

- I^2C x2
- I^2S
- UART x6
- Secure Digital
- SPI x3
- USB OTG LS/FS/HS
- CAN x2
- USB Charger Detect
- IEEE 1588 Ethernet
- USB Voltage Regulator

HMI

- GPIO
- Hardware Touch-Sensing Interface

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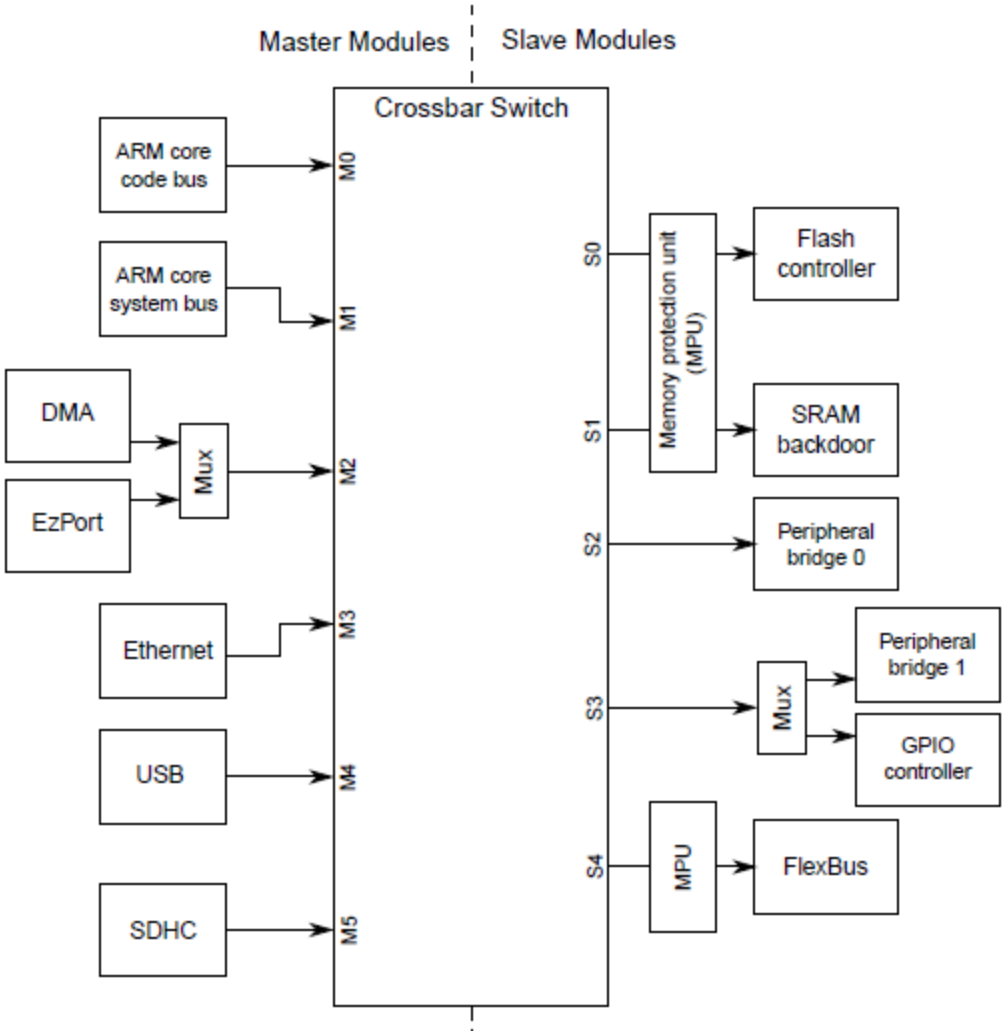
New Kinetis MCUs - Cross Bar Bus Switch (XBS)



Topic	Related module
Full description	Crossbar switch
System memory map	
Clocking	
Crossbar switch master	ARM Cortex-M4 core
Crossbar switch master	DMA controller
Crossbar switch master	EzPort
Crossbar switch master	Ethernet
Crossbar switch master	USB
Crossbar switch master	SDHC
Crossbar switch slave	MPU
Crossbar switch slave	SRAM backdoor
Crossbar switch slave	Peripheral bridges
Crossbar switch slave	GPIO controller
Crossbar switch slave	FlexBus

XBS, Cross Bar Bus Switch example (K60)

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New Kinetis MCUs - Memory Protection Unit (MPU)

- ✓ Provides memory protection and task isolation in multi-master platform
- ✓ Concurrently monitors all bus transactions for up to 8 AHB slave connections
  - ✓ Memory references with sufficient access control rights are allowed to complete
  - ✓ References not mapped to any region descriptor or with insufficient rights are terminated with a protection error response
  - ✓ 64-bit error register for each AHB slave port - capture the last faulting address, attributes and "detail" information
- ✓ Up to 16 region descriptors, each 128 bits in size
  - ✓ Granularity for region sizes from 32 bytes to 4 Gbytes
  - ✓ Two types of access control definitions
    - ✓ 4 bus masters support the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses
    - ✓ 4 bus masters support {read, writes} attributes
  - ✓ Region descriptor valid bit removes coherency issues associated with descriptor
  - ✓ Access rights of a descriptor can be altered dynamically via alternate memory view of access control word
  - ✓ For overlapping region descriptors, priority is given to *permission granting over access denying*

Pioneer Protected Resources

- ✓ TCMU System RAM
- ✓ TCML System RAM
- ✓ System RAM via crossbar slave port
- ✓ Flash
- ✓ FlexBus
- ✓ Three crossbar slave ports configured for the DDR Controller
- ✓ AIPS Resources not protected with MPU
  AIPS Resource have simplified protection scheme

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New Kinetis MCUs - Flash Security

Flash Security State

Security State	Description
Unsecured	Debug Access: Full FSL Factory Access: Full
Secured Level I	Debug Access: Mass Erase Only FSL Factory Access: ERSALL, RD1ALL, RDREG, WRREG, and the RAM-only commands
Secured Level II	Debug Access: Mass Erase Only FSL Factory Access: Mass Erase Only
Secured Level III	Debug Access: No Access FSL Factory Access: No Access

Change Flash Security State

Mechanism	Description
Backdoor Key	Providing an 8-byte key that is compared with one stored in flash allow the SW to change the security state. Usually the key is provided through an external port.
Debug Access	Through the debug port a Flash mass erase can be performed, clearing the security state.
FSL Factory Access	In secured Level I, NVMBIST mode can only perform a Mass Erase. Other test modes have full access to change all flags, and the entire contents of the NVM memory.

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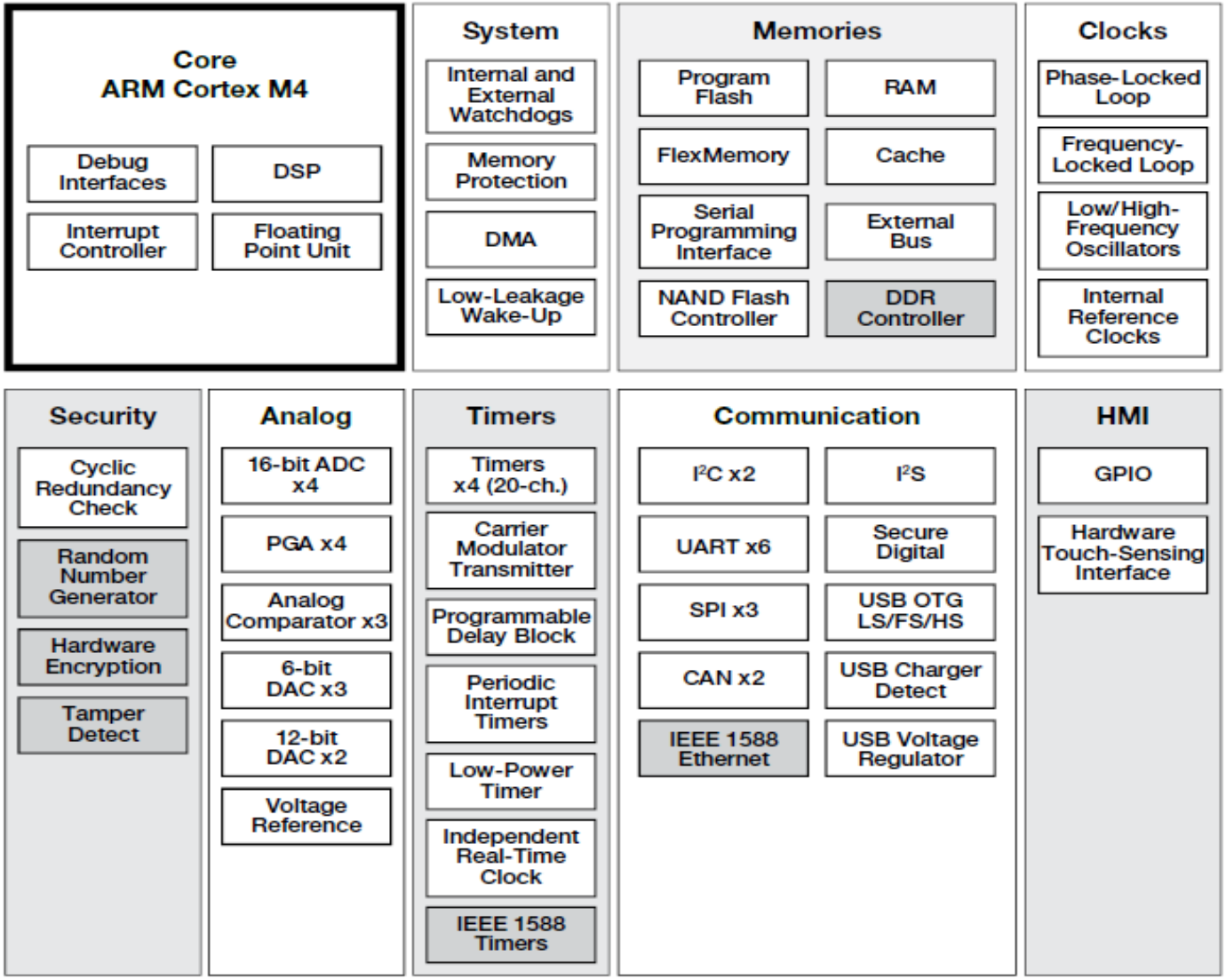
New Kinetis MCUs - Overview (K60)



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New Kinetis MCUs - Overview (K60)

Enhanced GPIO

- ✓ 5V tolerant pins on *some* devices
- ✓ Use open drain connections to interface to other 5V devices
- ✓ Pin interrupt and DMA capability
  - ✓ Rising/Falling edges and both edge and level
  - ✓ Each 32 pin port can generate an interrupt or DMA request
- ✓ Digital glitch filter
  - ✓ Spurious noise filter
  - ✓ Configurable width and clock source
- ✓ Hysteresis and configurable pull up/pull down device on all input pins
- ✓ Configurable slew rate and drive strength on all output pins
  - ✓ Reduced noise on output pins

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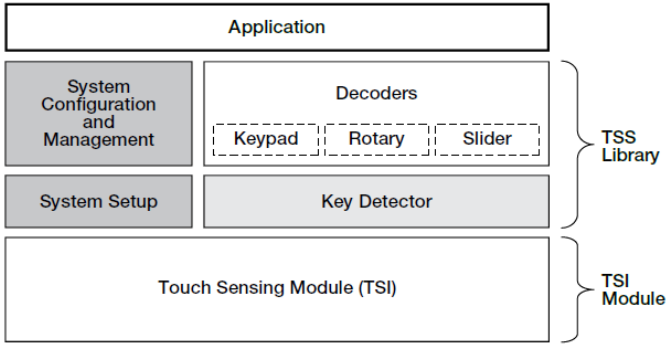
Touch Sense Interface (TSI)

Touch Sense Interface (TSI):

- ✓ Capacitive touch sensing detection across all low power modes
  - ✓ Automatic periodic scan with configurable duty cycle
  - ✓ Low power mode current adder can be <1uA
- ✓ 16 input capacitive touch sensing pins
  - ✓ Each with individual result registers
  - ✓ Automatic detection of Electrode Capacitance Change with programmable upper and lower threshold
- ✓ TSI interrupts
  - ✓ End of Scan, Out of Range, pad short or conversion overrun

Freescale provides a complete touch solution with a touch-sensing module that is seamlessly integrated with the Freescale Touch Sensing Library.
www.freescale.com/touchsensing



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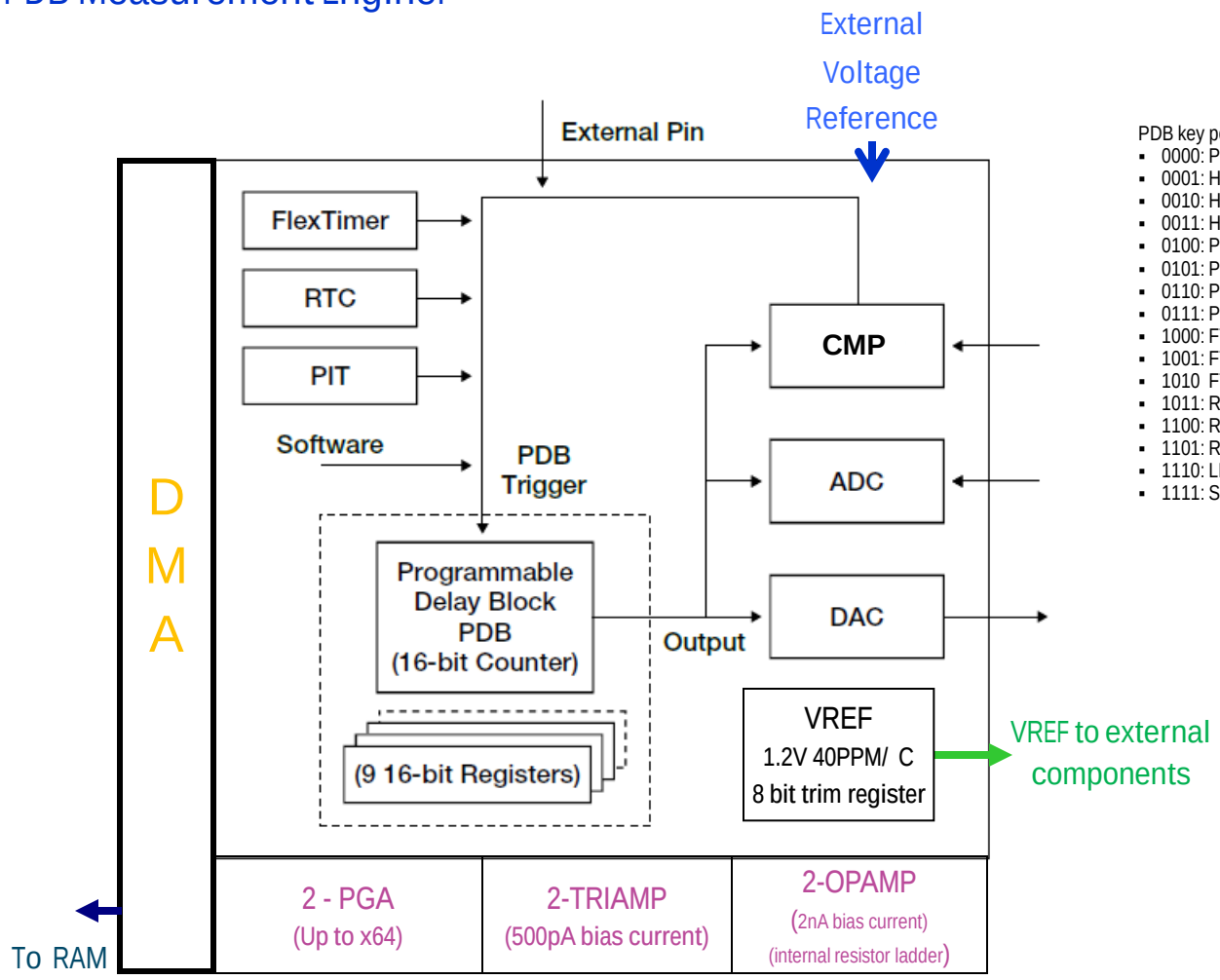
New Kinetis MCUs - Overview (K60)

DMA PDB Measurement Engine:



PDB key points: User Programmable PDB Trigger Sources

- 0000: PDB0_EXTRG pin - external pin connection
- 0001: HSCMP0 Output - module to module connection
- 0010: HSCMP1 Output - module to module connection
- 0011: HSCMP2 Output - module to module connection
- 0100: PIT Ch.0 Output - module to module connection
- 0101: PIT Ch.1 Output - module to module connection
- 0110: PIT Ch.2 Output - module to module connection
- 0111: PIT Ch.3 Output - module to module connection
- 1000: FTM0 Init Trigger Output - module to module connection
- 1001: FTM1 Init Trigger Output - module to module connection
- 1010 FTM2 Init Trigger Output - module to module connection
- 1011: Reserved
- 1100: RTC Alarm - module to module connection
- 1101: RTC Seconds - module to module connection
- 1110: LPT Output - module to module connection
- 1111: Software Trigger - self contained

Dynamic and Static Biasing

- Low temperature drift output
- Trimmed output
- Selectable voltage reference
- Current drivers

Signal Conditioning

- Trans-impedance amplifier
- Low pass Filter
- Unity gain buffer
- Gain amplifier

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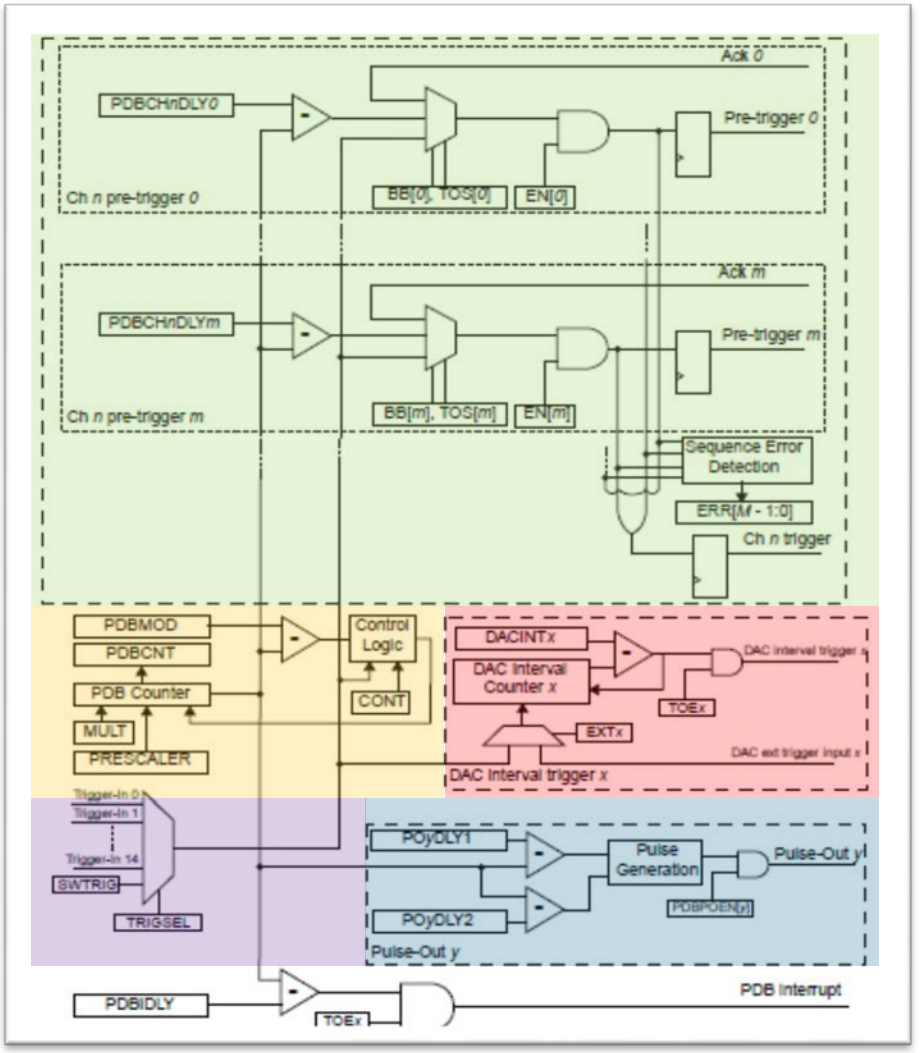
New Kinetis MCUs - Overview (K60)

DMA PDB Measurement Engine:

Programmable Delay Block (PDB) blocks:

- ✓ ADC pre-trigger and trigger generators 2 channels (1 for each ADC). Each channel with 2 pre-triggers note: ADC1 channel also routed to synchronous input of FTM0
- ✓ DAC interval timer 1 channel for DAC12
  (1ch, 2 triggers per channel one for each DAC)
- ✓ PDB delay counter
  The main reference counter in the PDB
- ✓ Pulse generator for CMPx
  1ch for all the CMPx. Generates windowing pulses
- ✓ Input trigger selector
  In current silicon the PDB has 14 input triggers form various peripherals (CMP, PIT, FTM, RTC, LPT) plus a sw trigger source.
  Activation of the selected trigger will reset and restart the main PDB delay counter
- ✓ PDB can also generate INT or DMA requests at any point of the trigger timing sequence



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New Kinetis MCUs - Overview (K60)

DMA PDB Measurement Engine:

Up to 3 Comparators (CMPx):

CMP:

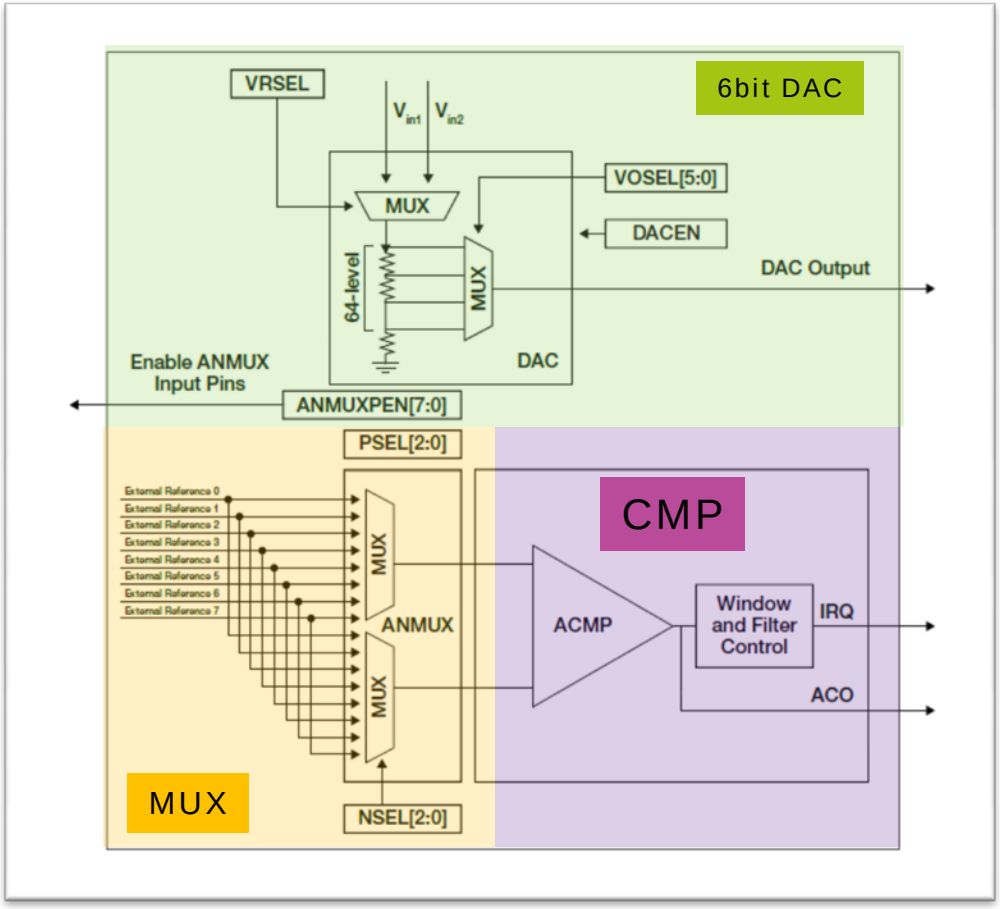
- ✓ Continuous, Sampled, Windowed modes
- ✓ Programmable filter and hysteresis

MUX:

- ✓ Up to eight independently selectable channels for positive and negative comparator inputs
- ✓ External pin inputs and several internal reference options including 6bDAC, 12bDAC, bandgap, VREF, OpAmp, TRIAMP

6bit DAC:

- ✓ Output range (Vin/64) to Vin
- ✓ VREF or VDD selectable as DAC



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DMA PDB Measurement Engine:

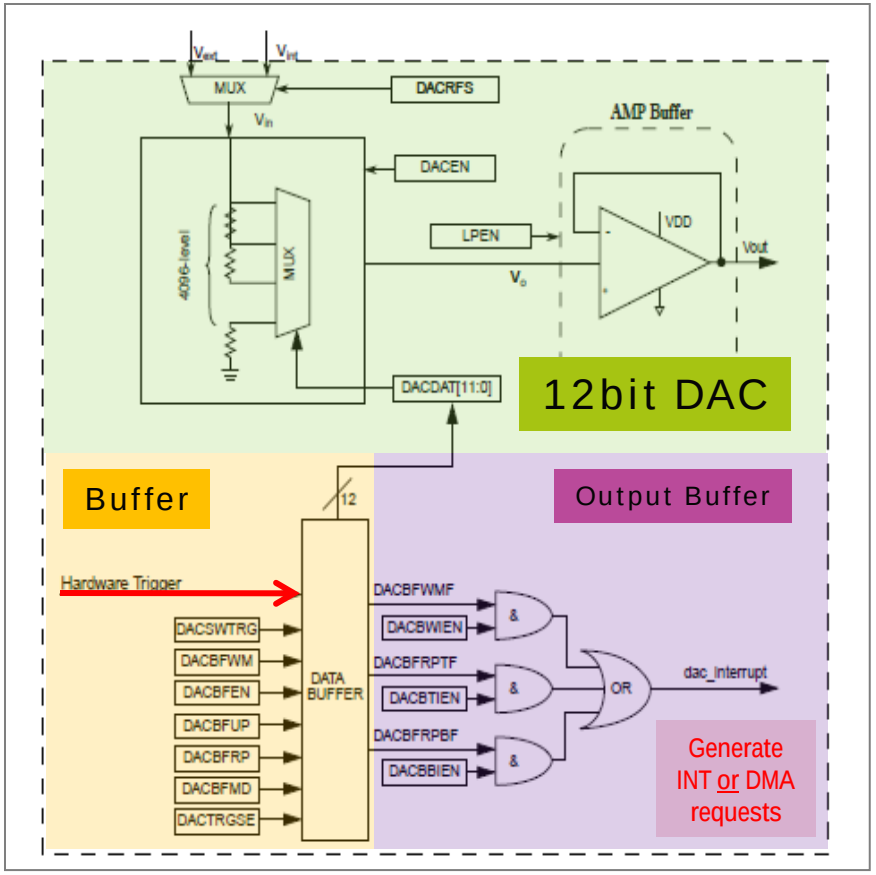
Buffer:

- ✓ PDB connects to DAC HW trigger

12bit resistive DAC:

- ✓ Selectable Reference Voltage
  - ✓ VDDA Pin (external)
  - ✓ VREF0 (VREF Module)

- ✓ Output to external pin or internal connection to other peripherals: Pins, ADCs, CMPs, OPAMP
- ✓ Operation in stop modes
- ✓ Multiple hardware interrupt & DMA request sources: Top or bottom positions or watermark
- ✓ DAC Modes:
  - ✓ Non-Buffered Mode
  - ✓ Buffered-Mode (Normal-/Swing-/One-Time- Scan Mode)



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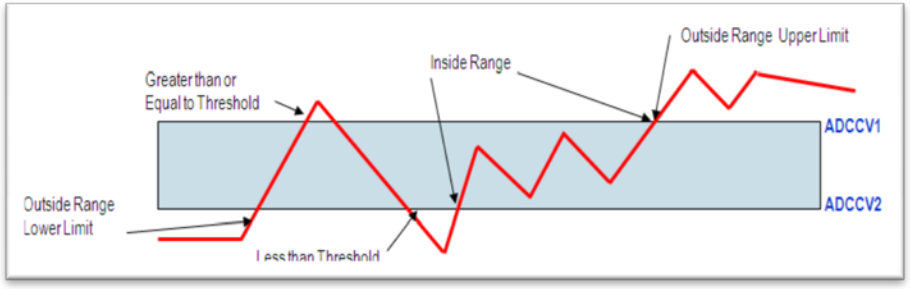
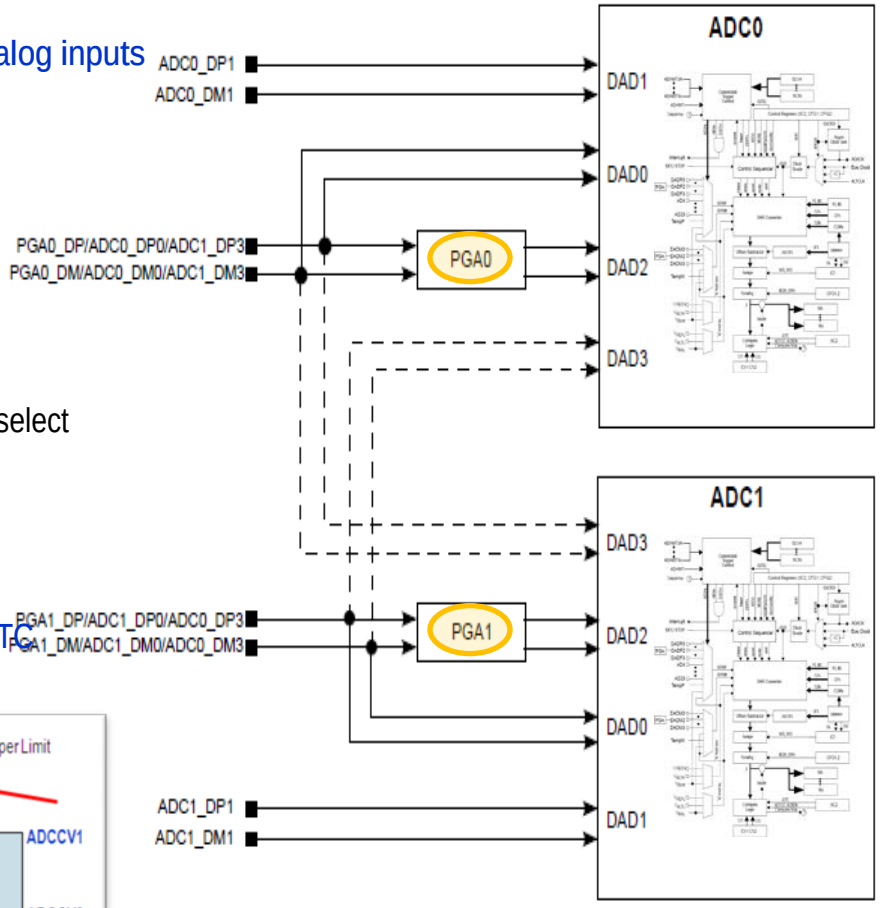
New Kinetis MCUs - Overview (K60)

16bit SAR architecture:

- ✓ Up to 4 pairs of differential and 24 single-ended external analog inputs
- ✓ Single or continuous conversion
  (*automatic return to idle after single conversion*)
- ✓ Configurable sample time and conversion speed/power
- ✓ Input clock selectable from up to four sources
- ✓ Operation in low power modes
- ✓ Asynchronous clock source for lower noise operation
- ✓ Selectable hardware conversion trigger with hardware channel select
- ✓ Hardware average function
- ✓ Self-calibration mode
- ✓ Programmable Gain Amplifier (PGA)
- ✓ Hardware trigger CMP0-3, PIT0-3, FlexTimer0-2, LPT, and RTC
- ✓ Automatic compare with interrupt





PGA gain [=1, 2, 4, 8, 16, 32, 64]

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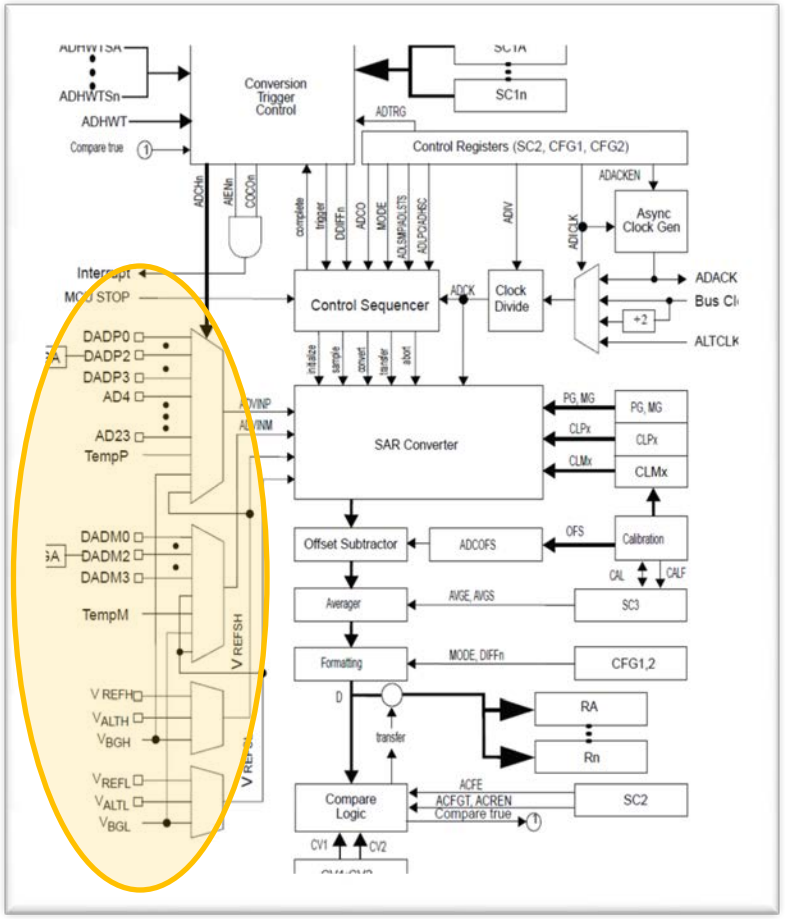
New Kinetis MCUs - Overview (K60)

16bit SAR architecture:

- ✓ Up to 24 single ended channels and 4 differential channels
- ✓ Internal channel connections from
  - ✓ DAC
  - ✓ Temp Sensor
  - ✓ PMC Bandgap
  - ✓ Vrefh, Vrefl
  - ✓ Vref_Out
  - ✓ Op-Amps*
  - ✓ Tri-Amps*

  * = K5x devices only
- ✓ VREF selection from:
  - ✓ Vrefh,Vrefl external pin pair or
  - ✓ VREF module
- ✓ Channel Interleaving on s.e and diff. channels



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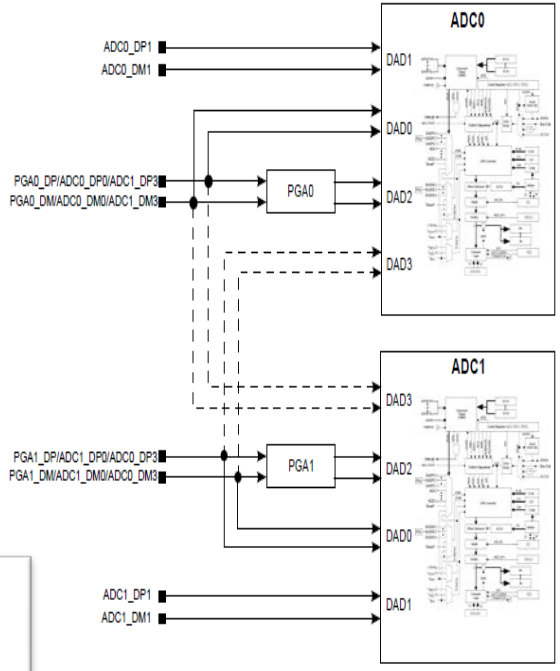
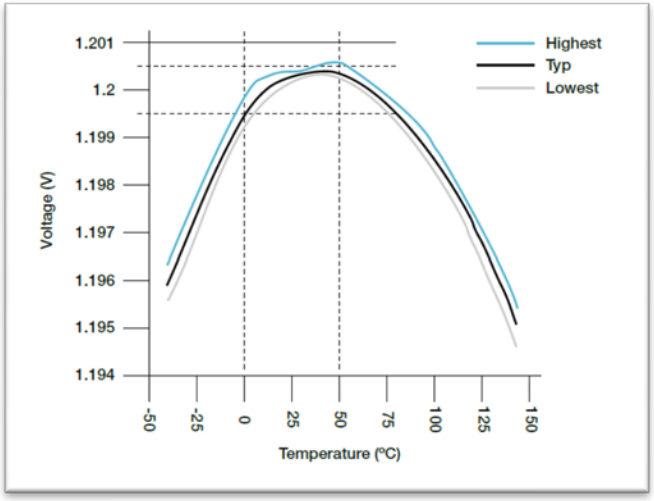
New Kinetis MCUs - Overview (K60)

16bit SAR modes:

- ✓ 8/10/12/16 bit Single Ended
- ✓ 9/11/13/16 bit Differential
- ✓ Single or Continous conversion
- ✓ Software or Hardware trigger
- ✓ Hardware averaging (4-32)
- ✓ End of conversion flag / interrupt / dma request
- ✓ Low Power - Normal mode
- ✓ Long or Normal sample time (4 Long time selections)
- ✓ Normal or High-Speed operation
- ✓ Compare function (Range or Tresholds)
- ✓ Clock selecton
- ✓ Vref selection





The voltage reference (VREF) is intended to supply an accurate voltage output that is trimmable by an 8-bit register in 0.5 mV steps. Temperature variation less than 33 ppm/C from 0o to 50oC.

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New Kinetis MCUs - Overview (K60)

FlexTimer

Buffered and write protection for critical registers.

- ✓ Up Free-Running
- ✓ Up (with inital value) and Signed Counting
- ✓ Input Capture (with glitch filtering) [ch0, ch1, ch2, ch3]
  [rising, falling, & both edges with optional input filter for some channels]
- ✓ Output Compare
  [output can be set, cleared, or toggled on match]
- ✓ Edge- or Centre-aligned PWM
  [double buffered PWM modulo and PWM value registers]
- ✓ Testing of input captures for a stuck at zero and one conditions
- ✓ Dual edge capture for pulse and period width measurement
- ✓ Hardware, Software and Channel Trigger
- ✓ Combine and Complementary
- ✓ Output Mask, Inverting, ...
- ✓ Motor control functions
  - ✓ Up to 4 fault detect inputs
  - ✓ Dead timer insertion
  - ✓ Quadrature Decoder
- ✓ DMA Mode
  [FTM0: CH0…CH7, FTM1: CH0/CH1, FTM2: CH0/CH1]

Support for motor control , power management, and digital lighting solutions

FTM is based/backwards compatible with HC9S08 TPM but with several key enhancements

[*signed up counter, deadtime insertion, fault inputs, enhanced triggering function, initialization and polarity*]

FTM instance	Number of channels	Features/usage
FTM0	8	3-phase motor + 2 general purpose or stepper motor
FTM1	2	Quadrature decoder or general purpose
FTM2	2	Quadrature decoder or general purpose

NOTE

The FTM1 and FTM2 configuration differs from the FTM0 configuration by reduced number of channels and by adding support for quadrature decoder mode.

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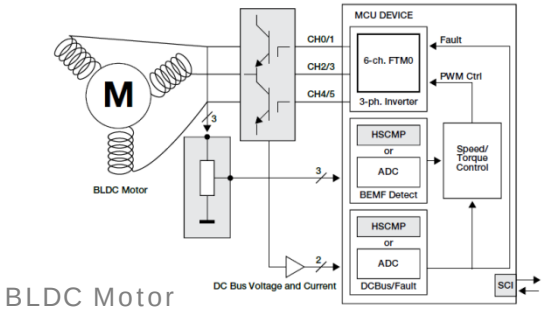
New Kinetis MCUs - Overview (K60)

FlexTimer

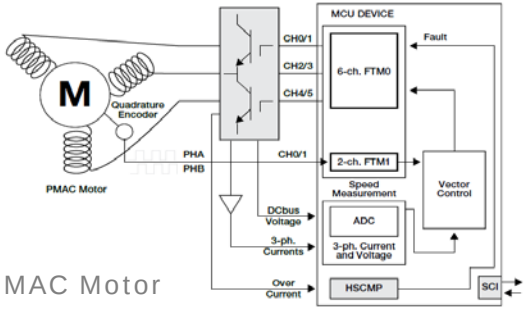
- ✓ Independently controllable PWM output polarity
- ✓ Up to four fault inputs can be assigned to control multiple PWM outputs
- ✓ Multiple interrupt sources

  Generation of an interrupt per channel, counter overflows, fault condition is detected
- ✓ Write protection for critical registers
- ✓ Temperature Sensor
- ✓ Glitch filter option
- ✓ Quadrature decoder with input filters,

  relative position counting and interrupt on position count or capture of position count on external event
- ✓ Global Time Base mode shares single time base across multiple FTM instances
- ✓ Testing of input captures for a stuck at zero and one conditions



BLDC Motor



PMAC Motor

The FlexTimer module (FTM) is designed for motor control and power management applications but also retains standard timer features, such as output compare or input capture functions.

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New Kinetis MCUs - Overview (K60)

PIT & LPT

Periodic Interrupt Timer (PIT):

4 x 32-bit timers, each contains:

- ✓ Programmable timeout periods
- ✓ Up to 4 mask able interrupts
- ✓ DMA trigger for the first 4 DMA channels
  (cycle / automatic mechanism without CPU intervention)

Common uses:

- *Time base for RTOS task scheduler*
- *Trigger source for ADC conversion+Trigger source for PDB*
- *Periodci trigger event for DMA channels*

DMA Channel Number	PIT Channel
DMA Channel 0	PIT Channel 0
DMA Channel 1	PIT Channel 1
DMA Channel 2	PIT Channel 2
DMA Channel 3	PIT Channel 3

Provide an automatic mechanism to transmit bytes, frames or packets at fixed intervals without the need for processor intervention.

Low Power Timer (LPT):

- ✓ 16bit counter (Free-runing, Pulse counter with compare [*rising or falling edge*])
- ✓ Selectable clock for prescaler / glitch filter (1kHz LPO, EXTAL, EXTAL32)
- ✓ Configurable Glitch Filter or Prescaler
- ✓ Interrupt or Reset generated on Timer Compare
- ✓ Hardware trigger generated on Timer Compare (not usable in low leakage modes)
- ✓ Hardware Trigger (Trigger HW events in other peripherals without SW intervention)

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New Kinetis MCUs - Overview (K60)

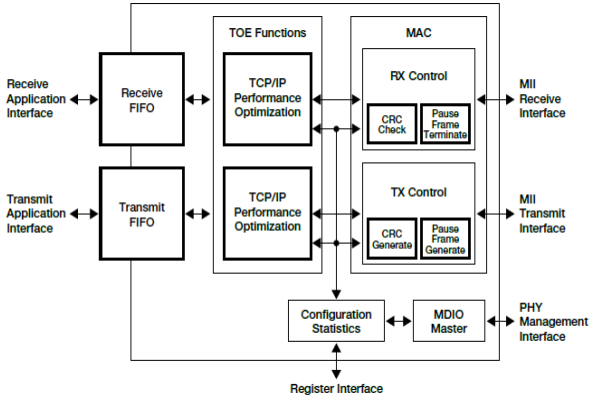
Communication (Ethernet, FlexCAN, SCI, DSPI, IIC, … USB)

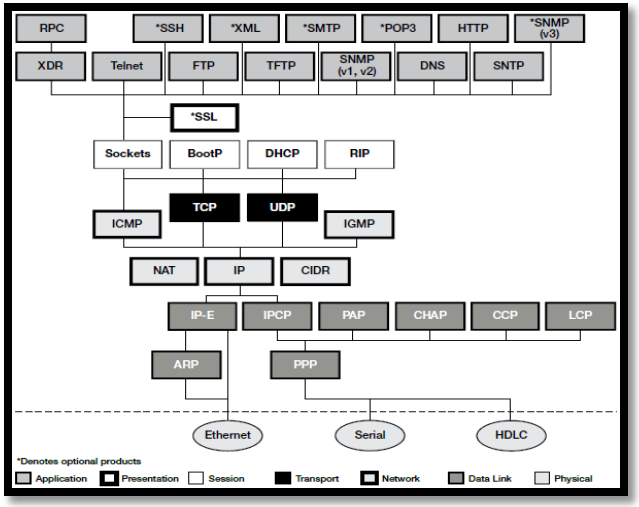
IEEE® 1588 Ethernet Controller:

The Ethernet controller module, in conjunction with an external 10/100 Ethernet PHY, is used to add Ethernet connectivity. Hardware IEEE 1588 time stamping provides precision clock synchronization for real-time control in networked automation, test and measurement applications.

Features of the Ethernet controller include:

- ✓ Full implementation of the 802.3 specification
- ✓ Supports MII and RMII interfaces to external PHY
- ✓ Supports Advanced Micro Devices (AMD) Magic Packet detection
  This utility allows an external node to make a remote wake-up request..
- ✓ Support for VLAN-tagged frames (IEEE 802.1Q)
- ✓ IP protocol performance optimizations:
  - Support for TCP/IP, UDP/IP, ICMP/IP and IP header-only protocols in IPv4 and IPv6 formats
  - Automatic IP header and payload (protocol specific) checksum generation and calculation
  - Transparent passing of frames of other types and protocols
- ✓ Hardware time stamping support for IEEE 1588





MQX RTOS : RTCS TCP/IP Stack

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New Kinetis MCUs - **NanoSSL™/ NanoSSH™ Client**

NanoSSL™/ NanoSSH™ Client for Freescale MQX Security options with significant cost savings

Secure Shell (SSH)

… encrypts communications between hosts over an insecure network, and it's great for logging into and executing commands on networked computers. It's also useful for tunneling, port-forwarding and secure file transfers using the SFTP protocol.

Secure Sockets Layer/Transport Layer Security (SSL/TLS)

… authenticates endpoints and encrypts channels to provide session privacy and security on the Internet. The standard operates at a higher level in the OSI stack than IPsec, and supports peer negotiation for algorithm selection, public key based exchange of secret session keys and X.509 certificates.

Freescale's super-fast, super-small embedded SSH/SSL client by Mocana

- ✓Ultra-small at less than one fifth the size of a typical SSL/SSH client.
- ✓Minimal impact on device performance
- ✓Minimal impact on flash ROM utilization

- **One-time "unlocking" fee of $199 to access source code with unlimited binary distribution**
- **Available via Buy Direct** www.freescale.com/embeddedcomponents

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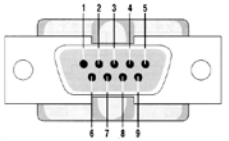
New Kinetis MCUs - Overview (K60)

Communication (Ethernet, FlexCAN, SCI, DSPI, IIC, … USB)



Serial communication Interface (SCI / UART)

The serial communication interface (SCI) module allows for asynchronous, fullduplex serial communication in a variety of formats. Features of the SCI include:

- ✓ Standard mark/space non-return-to zero format (NRZ)
- ✓ Supports IrDA 1.4 return-to-zero inverted (RZI) format
- ✓ Supports ISO 7816 protocol for interfacing with SIM cards and smartcards
- ✓ 13-bit baud rate selection with by-32 fractional divide
- ✓ Programmable eight- or nine-bit data formats
- ✓ Ability to select MSB or LSB to be first on the wire
- ✓ Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- ✓ Separate TX and RX FIFOs with DMA request capability (*decrease CPU loading*)

SCI Instance	Features	Maximum Baud Rate
SCI0	Higher Baud Rates (CPUCLK @ 100 MHz) ISO-7816 8 TX and 8 RX FIFOs	6.25 Mbits/sec
SCI1	Higher Baud Rates (CPUCLK @ 100 MHz) 8 TX and 8 RX FIFOs	6.25 Mbits/sec
SCI2-SCI5	Normal Baud Rates (BUSCLK @ 50 MHz) No TX and RX FIFOs	3.13 Mbits/sec

*SCI baud rate = SCI module clock / (16 * (SBR[12:0] + BRFD)*

Reduced CPU Loading

- ✓Rx, Tx from UART can assert DMA request
- ✓UART0, UART1 have 8-entry Rx, Tx FIFOs
- ✓All UARTs have optional RTS, CTS
- ✓UART2-5 have double-buffered registers

Address-Match feature for Low Power enablement

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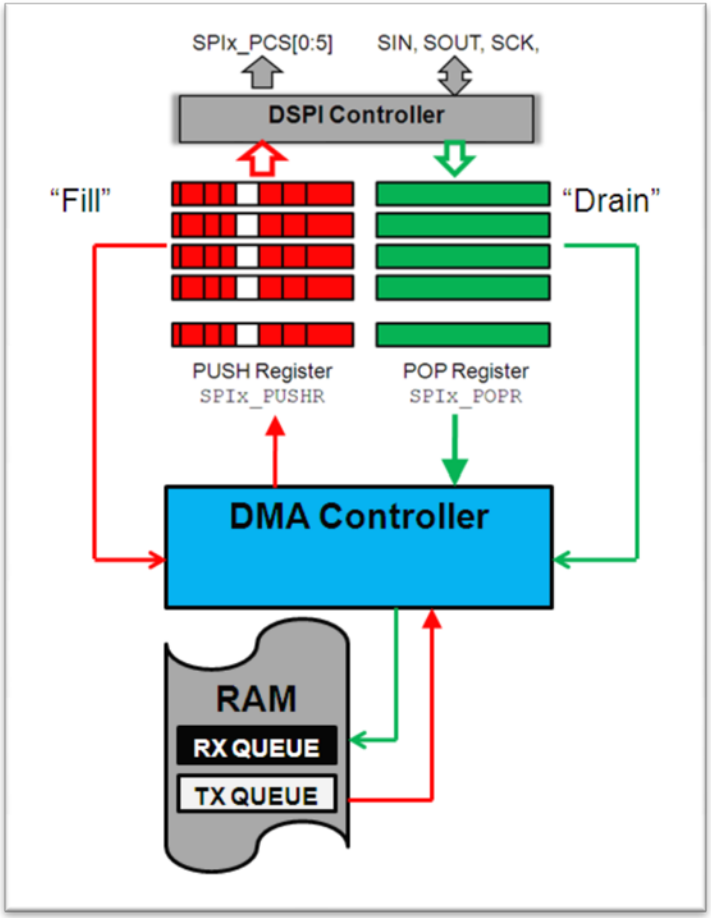
New Kinetis MCUs - Overview (K60)

Communication (Ethernet, FlexCAN, SCI, DSPI, IIC, … USB)

'DMA' Serial Peripheral Bus (DSPI)

A 3 wire, full duplex synchronous bus, features of the DSPI:

- ✓ 3 SPIs on 144pin packages
  - Max Master speed is fBUS/2 = 25MHz
  - Max Slave speed is fBUS/4 = 12.5MHz
- ✓ 2 FIFOs, each 4 level deep [with debugger access]
  - Transmit FIFO & Push Register
  - Receive FIFO & Pop Register
- ✓ DMA Capable "Queued Mode"
  - Command Buffer in system RAM
  - "Tx FIFO not full" DMA trigger
  - "Rx FIFO not empty" DMA trigger
- ✓ Up to 6 Peripheral Chip Selects
  (can be expanded with external mux)
- ✓ Muxed to several alternate ports
  (e.g. DSPI0 available on 3 ports for 144pin package)



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New Kinetis MCUs - Overview (K60)

Communication (Ethernet, FlexCAN, SCI, DSPI, IIC, … USB)

I²C Bus Interface

Standard I²C Features, of course:

- ✓ Multi-master operation
- ✓ 7-bit address or 10-bit address extension
- ✓ Software-selectable acknowledge bit
- ✓ Interrupt-driven byte-by-byte data transfer
- ✓ Arbitration-lost interrupt with automatic mode switching from master to slave
- ✓ Calling address identification interrupt
- ✓ START and STOP signal generation and detection
- ✓ Repeated START signal generation and detection
- ✓ Acknowledge bit generation and detection
- ✓ Muxed to several alternate ports
- ✓ e.g. I2C0 available on 3 ports for 144pin package

Advanced I²C Features:

- ✓ Address Flexibility:
  - Two programmable slave address match registers
  - One programmable slave address range register
- ✓ Address matching causes wakeup when the core is in stop mode:
  - *No peripheral bus running*
  - *Recognizes Primary, range or General Call addresses (if they are enabled)*
  - *Data is lost; I²C in slave mode*
- ✓ General call recognition (address: 0000000)
- ✓ Others:
  - *Programmable for one of 64 different serial clock frequencies*
  - *Supports System Management Bus (SMBus) Specification, version 2*
- ✓ DMA Support

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New Kinetis MCUs - Overview (K60)

Communication (Ethernet, FlexCAN, SCI, DSPI, IIC, … USB)

CAN

FlexCAN Interface

Standard I²C Features, of course:

- ✓ Compliant to CAN protocol Ver 2.0B
- ✓ Standard data and remote frames
- ✓ Extended data and remote frames
- ✓ Zero to eight bytes data length
- ✓ Programmable bit rate up to 1 Mb/sec
- ✓ Content-related addressing
- ✓ Flexible Mailboxes Architecture
  - 16 mailboxes
  - Zero to eight bytes data length
  - Each configurable as Rx or Tx
  - Individual Rx Mask Registers per Mailbox
  - Full featured Rx FIFO with storage capacity for up to 6 frames and automatic internal pointer handling

Advanced / NEW Features:

- ✓ Extended ID Filtering
- ✓ Safe mechanism for ID filter re-configuration
- ✓ Match incoming IDs against:
  - 128 extended IDs, or 256 standard IDs or
  - 512 partial IDs, with up to 32 individual masking capability
  - Flexible Mailboxes
  - Rx Mailboxes can be configured with the same acceptance criteria
    - Reception Queue
    - Allows the CPU more time to service received messages
  - Selectable priority of message reception between Mailbox and Rx FIFO

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New Kinetis MCUs - Overview (K60)

Communication (Ethernet, FlexCAN, SCI, DSPI, IIC, … USB)

Full Synchronous Serial Interface (SSI)

A full duplex synchronous bus (typical use case audio) :

- ✓ 1 SSI on 144pin packages
- ✓ Supports a variety of formats:
  - AC97
  - I2S
  - 'Normal' Modes
    - Synchronous, also Gate Clock mode
    - Asynchronous
  - Network (TDM) Mode
- ✓ FIFO Architecture
  - Dual 15-entry, 32-bit Transmit FIFOs
  - Dual 15-entry 32-bit Receive FIFOs
- ✓ DMA Capable
  - "Tx FIFOn empty" DMA trigger
  - "Rx FIFOn full" DMA trigger
- ✓ Optional internal clock or external input clock
- ✓ Muxed to several alternate ports
  (SSI available on 3 ports for 144pin package)

Full duplex serial port that allows communication with a variety of serial devices:

- o Audio codecs that implement the inter-IC sound bus (I2S)
- o Standard codecs
- o Digital signal processors (DSPs)
- o Microprocessors
- o Peripherals
- o AC97 support

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New Kinetis MCUs - Overview (K60)

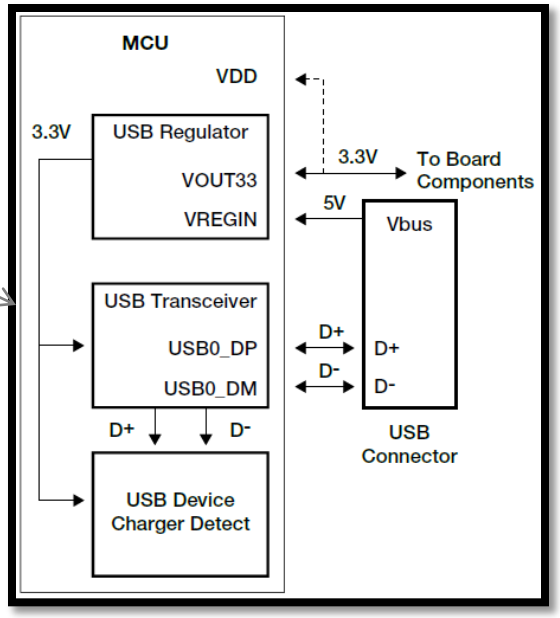
Communication (Ethernet, FlexCAN, SCI, DSPI, IIC, … USB)

USB

The USB subsystem is comprised of several blocks that together provide full, flexible USB functionality.

Options are:

- ✓ Full-speed (FS) / low-speed (LS) USB controller
- ✓ High-speed (HS)-capable controller (*Kinetis K20 and K60 families only*)
- ✓ On-chip FS/LS USB transceiver
- ✓ *USB regulator*
- ✓ *USB device charger detection*



USB Regulator Feature

5V regulator input (VREGIN) typically provided by USB Vbus or Rechargeable Battery power 3.3V regulated output powers on-chip USB transceiver and device charger detect.

Can be used to power external components or MCU main power supply with up to 120mA).

USB FS/LS Controller

The USB FS/LS controller provides USB host and device communications along with support for OTG operation.

The FS/LS controller is USB 2.0 compliant and supports full-speed (12 Mbps) and low-speed (1.5 Mbps) data transfer rates.

The FS/LS controller is always used with the on-chip FS/LS transceiver block. The on-chip transceiver includes internal pulldown resistors on the D+ and D- lines and an internal pullup resistor on the D+ line. This helps to reduce the number of external components needed for USB connectivity.

USB HS-Capable Controller

The USB HS-capable controller provides USB host and device communications along with support for OTG operation.

The HS-capable controller is USB 2.0 compliant. The controller supports highspeed (480 Mbps), full-speed (12 Mbps) device and OTG operation; The controller supports HS/FS/LS host operation.

The HS-capable controller can be used with an optional external UTMI+ low pin interface (ULPI) PHY to support HS mode.

If HS operation is not needed, then the on-chip FS/LS transceiver can be used instead.

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New Kinetis MCUs - Overview (K60)

Communication (Ethernet, FlexCAN, SCI, DSPI, IIC, … USB)

Ehanced Secure Digital Host Controller (eSDHC)

- ✓ Card bus clock frequency up to 50 MHz
- ✓ Supports
  - ✓ *1-bit / 4-bit SD and SDIO modes*
  - ✓ *1-bit / 4-bit / 8-bit MMC modes*
  - ✓ *1-bit / 4-bit / 8-bit CE-ATA devices*
- ✓ Up to 200 Mbps of data transfer for SD/SDIO cards using 4 parallel data lines
- ✓ Up to 416 Mbps of data transfer for MMC cards using 8 parallel data lines in SDR(Single Data Rate) mode
- ✓ Supports Single Block, Multi Block read and write
- ✓ Supports block sizes of 1 ~ 4096 bytes
- ✓ Supports the write protection switch for write operations
- ✓ Supports both synchronous and asynchronous abort (both hardware and software CMD12)
- ✓ Supports pause during the data transfer at block gap
- ✓ Supports SDIO Read Wait and Suspend Resume operations
- ✓ Supports Auto CMD12 for multi-block transfer
- ✓ Host can initiate non-data transfer command while data transfer is in progress
- ✓ Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes, also supports interrupt Period
- ✓ …
- ✓ Embodies a fully configurable 128x32-bit FIFO for read/write data
- ✓ Supports internal and external DMA capabilities
- ✓ Supports voltage selection by configuring vendor specific register bit
- ✓ Supports Advanced DMA to perform linked memory access

eSDHC Modes of Operation

SD	MMC		CE-ATA	SD/SDIO
SD 1-bit	MMC 1-bit	Identification Mode (up to 400 kHz)	CE-ATA 1-bit	SD/SDIO full speed mode (up to 25 MHz)
SD 4-bit	MMC 4-bit	MMC full speed mode (up to 20 MHz)	CE-ATA 4-bit	SD/SDIO high speed mode (up to 50 MHz)
	MMC 8-bit	MMC high speed mode (up to 52 MHz)	CE-ATA 8-bit	

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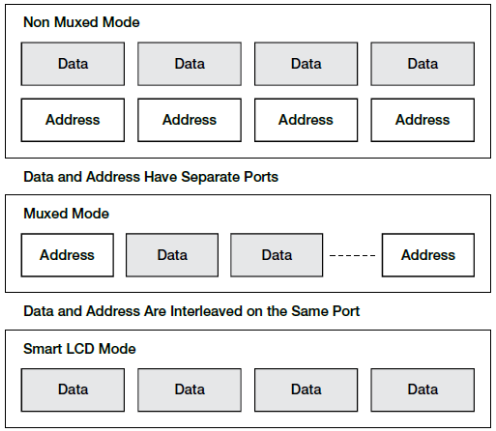
New Kinetis MCUs - Overview (K60)

Mini FlexBus/FlexBus, NAND-CTRL (NFC) and DRAM-CTRL



FlexBus Modes of Operation

NAND Flash Interface: 8bit / 16bit:

- ✓ Memory mapped Registers and SRAM buffer
- ✓ Supports all NAND Flash products regardless of density/organization (with page size of 512+16B/2K+64B/4K+128B/4K+218B/8K)
- ✓ Configurable 2 DMA channels
  - Use DMA channel 1 to read/write the main area of a page, and DMA channel 2 for the spare area
  - Use DMA channel 1 only to read/write a page for both main and spare area of a page

DRAM Interface: 8bit / 16bit:

- ✓ Maximum Frequency (Clock/Data) 125/250 MHz
- ✓ Memories Types Supported: DDR, DDR2, LPDDR
- ✓ Support up to 512MByte of external memory
- ✓ Fully Asynchronous operation with an independent PLL
- ✓ Supports low-power modes

Secure Boot
Device boot exclusively from Flash.

Mini FlexBus/FlexBus:

- ✓ Designed to connect up to six external devices (Mini FlexBus / FlexBus)
- ✓ Each version has 8bit, 16bit and 32bit port size with configuration for multiplexed or non-multiplexed addresses and data buses
- ✓ FlexBus is a very flexible interface that supports: Flash, Smart LCDs, FPGAs, SRAM, PROM, EPROM, EEPROM

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New Kinetis MCUs - Overview (K60)

MMCAU, RNGB and CRC

Cryptographic Acceleration Unit (CAU):

Accelerates the following encryption algorithms: DES, 3DES, AES, MD5, SHA-1, SHA-256

Pseudo-Random Number Generator (RNGB):

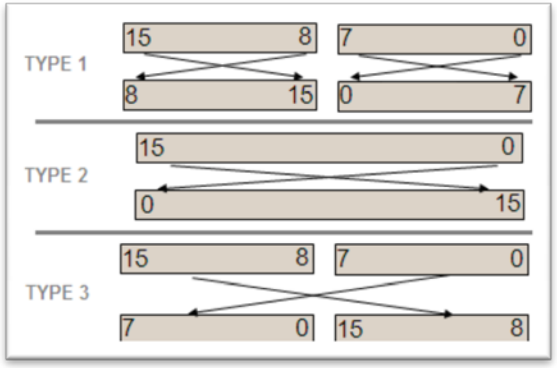
National Institute of Standards and Technology (NIST)-approved PRNG: http://csrc.nist.gov

Supports the key generation algorithm: http://www.itl.nist.gov/fipspubs/fip186.htm

Integrated entropy sources capable of providing the PRNG with entropy for its seed.

Hardware Cycle Redundancy Check Generator support 16-bit & 32bit (CRC):

- ✓ Programmable initial seed value and Polynomial.
- ✓ Support transpose input data and CRC result via transpose register (required for certain CRC standards).
- ✓ Support three types Transpose
- ✓ Final XOR of the output (Some CRCs have final XOR of their CRC checksum with 0xFFFFFFFF or 0xFFFF in their protocol)



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ARMv7-M Debug Features

Debug Interface Pins:

2-pin Serial Wire Debug (ARM SWD)

- SWD_CLK (available on JTAG_CLK pin)
- SWD_DIO (available on JTAG_MS pin)

4- pin or 5-pin JTAG

- JTAG_CLK
- JTAG_DO
- JTAG_DI
- JTAG_MS
- *JTAG_TRST (optional JTAG Reset)*

2-pin cJTAG

- JTAG_CLK
- JTAG_MS

- JTAG is the default debug mode from MCU Power-on Reset (POR)
- To enter SWD or cJTAG debug modes the debugger must shift a sequence on TCLK and TMS pins
- After SWD or cJTAG debug modes are entered, DO pin can be used as TRACE_SWO or other function and DI pin can be used for other function

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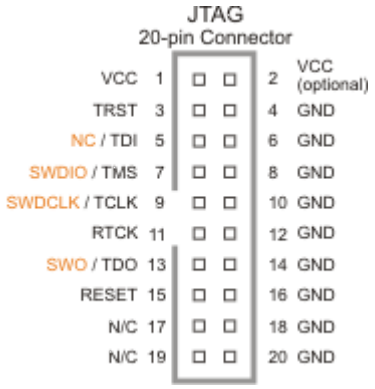
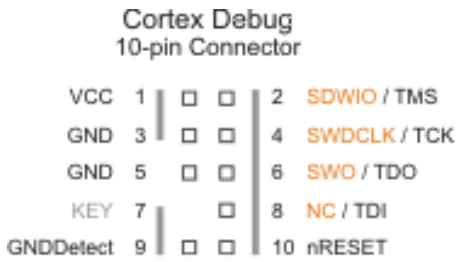
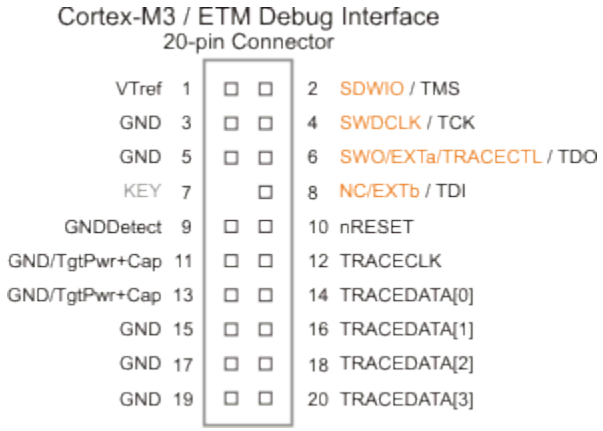
ARMv7-M Debug Features - Debug & Trace Connectors



Planned Adapter from ARM Standard JTAG Connector to Cortex Debug Connector





Planned Connectors for Pioneer Development Tools

- **20-pin (0.10") - ARM Standard JTAG Connector**
- **10-pin (0.05") - Cortex Debug Connector**
- **20-pin (0.05") - Cortex Debug+ETM Connector**

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Choose Your Partner: The Freescale MCU Ecosystem

Run-Time Software: RTOS, Stacks, File System

Embedded Access Inc | freescale semiconductor | Green Hills Software | expresslogic | SEGGER | Micrium | freeRTOS | CMX Systems | CMSIS Compliant | Quadros Systems Inc.

ARM® Cortex™ Microcontroller Software Interface Standard - hardware abstraction layer

HW BDM Debugger/Emulators

PE micro | IAR Systems | SEGGER | RAISONANCE | Rowley Associates | KEIL An ARM® Company | LAUTERBACH DEVELOPMENT TOOLS | SIGNUM SYSTEMS

IDE: Tools Compliers, Debuggers

CodeWarrior | CodeSourcery | IAR Systems | KEIL An ARM® Company | GNU Tools | Green Hills Software

MQX Support / Design Services

EAI

Audio/Video Codecs

AllGo embedded

GUI Graphical

SEGGER | SWELL | eGUI

Security / Medical

mocana | monebo

EVBs & System Design

freescale semiconductor | IAR Systems | AXIOM | KEIL An ARM® Company

Ind. Protocol Stacks

IXXAT

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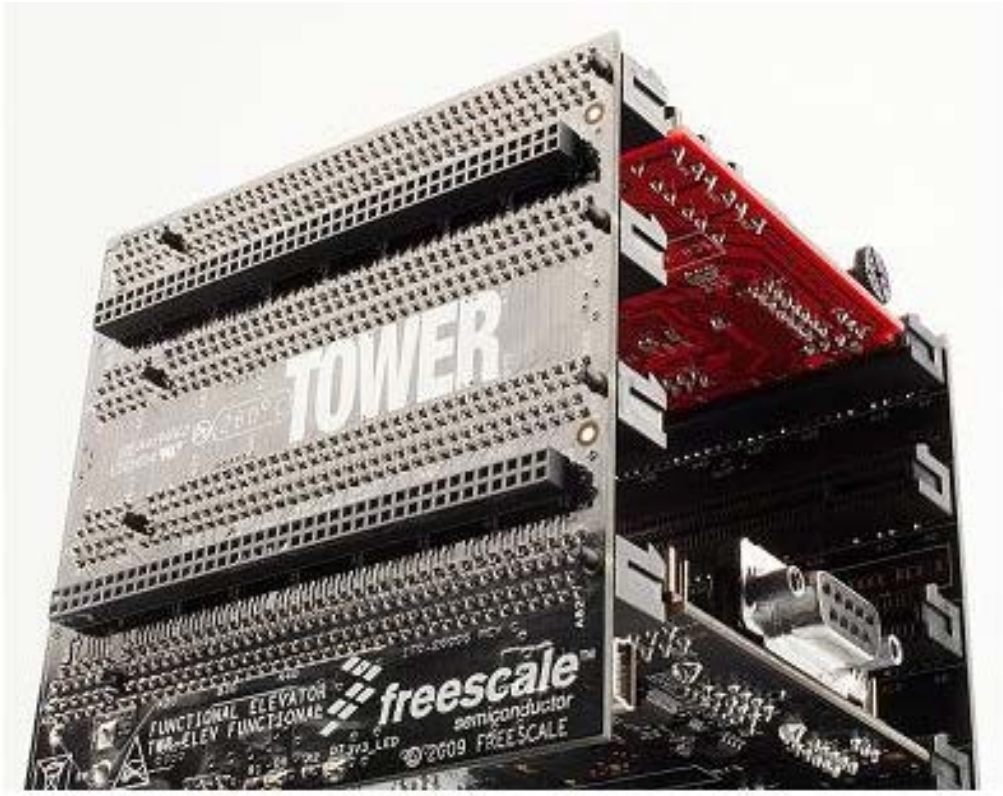
New Kinetis MCUs - Tower System

ARM® Cortex™-M4 MCUs



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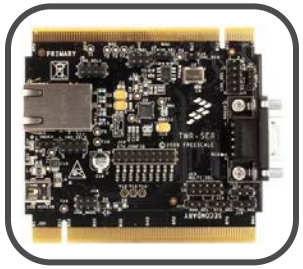
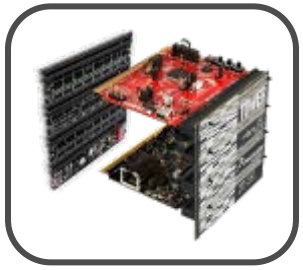
New Kinetis MCUs - Tool chain & 3rd Parties

ARM® Cortex™-M4 MCUs

Tower System





Choose a Microcontroller Module [DSC, ColdFire, MPC5121, MPC56xxP, Kinetis]

Choose a Peripheral Module

Connect each module to the Elevator Boards

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TWR - Tower System Modules

www.freescale.com/tower

Processor Modules ($39-$69)

TWR-MCF51CN

TWR-MCF5225X

TWR-S08LL64

TWR-MPC5125

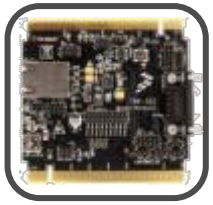
TWR-MCF51MM
TWR-S08MM128

New

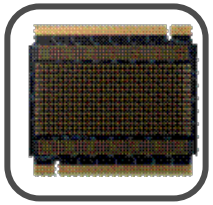
TWR-K60N512
TWR-K40X256
TWR-MCF5441X
TWR-MCF51AG
TWR-56F8257
...

Coming Soon

Peripheral Modules ($15 – $149)



TWR-SER



TWR-PROTO

TWR-ELEV

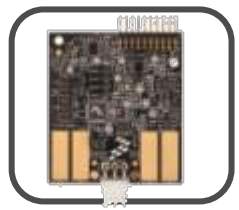
TWR-MEM

New

TWR-SENSOR-PAK

New

TWR-LCD



MED-EKG

Coming Soon

New

TWR-WIFI-RS2101

Wi-Fi 802.11b

TWR-WIFI-G1011MI

Analog Digital Converter

TWR-ADCDAC-LTC

Dual Ethernet & High-speed USB

TWR-SER2

Audio

TWR-AUDIO

Industrial Ethernet Module
PISMO Memory Expansion
Home Plug Powerline Comm
...

Under Development

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New Kinetis MCUs - Tower System

A modular development platform for 8/16/32-bit MCUs & MPUs

- Quickly combine Tower Modules to build a prototype of your application
- Modules sold individually or in kits
- Open Source: Build your own Tower Module to integrate your IP
- Cost-optimized hardware
- Software support from Freescale and Third Parties
- Growing community of Third Party hardware support
- On-line community: www.towergeeks.org

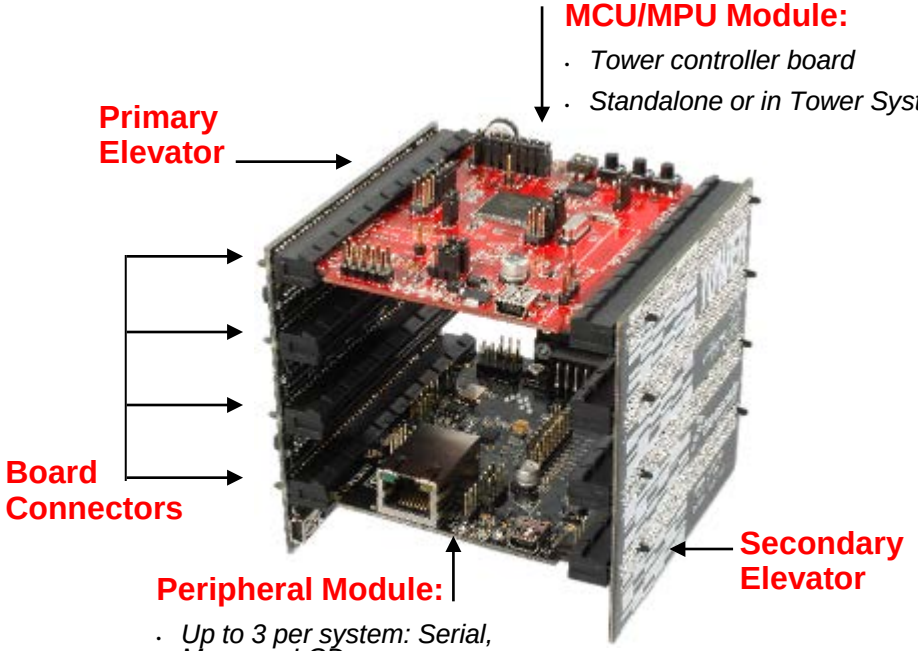
Part Number	Contents	Price (SRP)
TWR-K40X256	TWR-K40X256 module	*$59
TWR-K40X256-KIT	TWR-K40X256 module TWR-ELEV module TWR-SER module	*$129
TWR-K60N512	TWR-K60N512 module	*$59
TWR-K60N512-KIT	TWR-K60N512 module TWR-ELEV module TWR-SER module	*$129

TWR-MEM

TWR-LCD

TWR-SENSOR-PAK

Rapidly build a prototype of your end application



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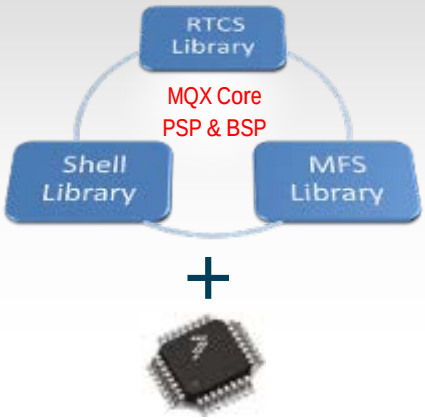
New Kinetis MCUs - Tower System

ARM® Cortex™-M4 MCUs

Freescale MQX + MCU

Free MQX RTOS



- Full-featured, scalable, proven RTOS
- Simplifies HW management, streamlines SW development
- Reduces development costs while speeding time to market

Comprehensive solution for embedded control and connectivity

+ Tower System

- Modular, expandable and cost-effective development platform for 8/16/32-bit MCUs and MPUs
- Rapid eval and prototyping with maximum HW reuse.
- Supported by a diverse range of MCU and peripheral plug-in boards and a growing web community

Open source hardware platform for prototyping application development

+ CodeWarrior *IDE*

- Eclipse environment
- Processor Expert code generation wizard
- Build, debug and flash tools
- Software analysis
- Kernel-aware debug
- Host platform support

Visual and automated framework to accelerate development time

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Freescale eGUI

www.freescale.com/eGUI

The complimentary Freescale embedded graphical user interface (eGUI) allows single chip microcontroller (MCU) systems to implement a graphical user interface and drive the latest generation of color graphics LCD panels with integrated display RAM and simple serial peripheral interface (SPI) or parallel bus interface. The evolution of LCD panels integrating the display RAM and LCD controller means that your products can easily be implemented without the need for a conventional microprocessor (MPU) with integrated LCD driver hardware and external display RAM. The eGUI has also been expanded to support conventional LCD panels and ColdFire LCD MPUs, giving a complimentary entry level solution for these platforms. To support the eGUI, Freescale also provides a "converter utility" to change graphical bit maps and fonts into the "C" language arrays needed by the eGUI.

The Freescale eGUI can be used stand alone or integrated into the MQX operating system.

Both Types of LCD Driving Methods supported

- ✓ Traditional LCD System (dedicated LCD MPU)
- ✓ SPI/Parallel driven LCD

- ✓ Multiple platforms supported: HCS08, HCS12, ColdFire, and planed for Kinetis
- ✓ Extremely low flash and RAM footprint
- ✓ Smart support for screen oriented structure of user code
- ✓ Supports LCD displays up to 1/4 VGA for MCU and larger for MPUs supported

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Freescale SWELL Software

Freescale acquired key assets of Swell Software on August 18, 2010, an industry leader in GUI software tools

- ✓ Swell Software provides Graphical User Interface (GUI) Solutions for Embedded Devices. The PEG family of tools are designed to meet widely varying power, performance and memory requirements. Helping our customers:
  - ❑ Reduce product development risk
  - ❑ Lower in-house development costs
  - ❑ Accelerate time to market
- ✓ PEG Software accelerates GUI design for embedded devices by allowing developers to create prototypes on a Windows or Linux-based PC by providing a complete visual layout and design tool to enable GUI design to take place in parallel to the embedded software/hardware development.
- ✓ The PEG WindowBuilder™ automatically generates C++ source code that is ready to be compiled and linked into any application, further accelerating the deployment of the final product.

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New Kinetis MCUs - **Cortex-M4 Math & DSP Libraries**

Free ARM Cortex-M4 Math & DSP libraries

- CodeWarrior, IAR, Keil, and CMSIS C callable and operating system independent functions
- Functions optimized for ARM Cortex-M4 using compiler intrinsics for DSP/SIMD instructions
- Separate functions for 8-bit, 16-bit, 32-bit integers and 32-bit floating-point values
- Supports many math and DSP functions:

Filtering
- Biquad cascade direct form 1 (IIR)
- Convolution
- Partial convolution
- FIR (transversal) filter
- Polyphase FIR decimator
- Polyphase FIR interpolator
- LMS adaptive filter
- Normalized LMS adaptive filter
- Sparse FIR filter
- Correlation
- 64-bit high precision biquad filters
- FIR lattice filters
- Direct form 2 transposed IIR filter
- IIR lattice filters

Transforms
- Complex forward FFT
- Real FFT
- Inverse real FFT
- Discrete cosine transform
- Inverse discrete cosine transform

Matrix addition, subtraction, transpose, scaling, inversion

Controller
- PID controller
- Field oriented control (clarke and park transforms)

Vector Math
- Absolute value
- Add (element by element)
- Vector dot product
- Multiply elements
- Invert sign (negate)
- Add constant offset
- Scale by constant
- Shift left/right
- Subtract (element by element)

Fast Math
- Sine, Cosine, Square root

Interpolation (linear and bilinear)

Complex Math
- Complex conjugate
- Complex magnitude
- Complex magnitude squared
- Complex by complex multiplication
- Complex by real multiplication
- Complex dot product

Statistics
- Maximum / minimum value
- Mean
- Power
- Root mean square (RMS)
- Standard Deviation
- Variance

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New Kinetis MCUs - Tool chain & 3rd Parties

ARM® Cortex™-M4 MCUs

www.iar.com/freescale

- ✓ **The most widely used tool chain for ARM MCUs**
- ✓ **A consistent tool chain for ColdFire+ and Kinetis devices**
- ✓ **Completely integrated development environment**
- ✓ **Highly optimized IAR C/C++ Compiler**
- ✓ **Powerful IAR C-SPY Debugger**
- ✓ **MQX integration**
- ✓ **Ready-made example projects**

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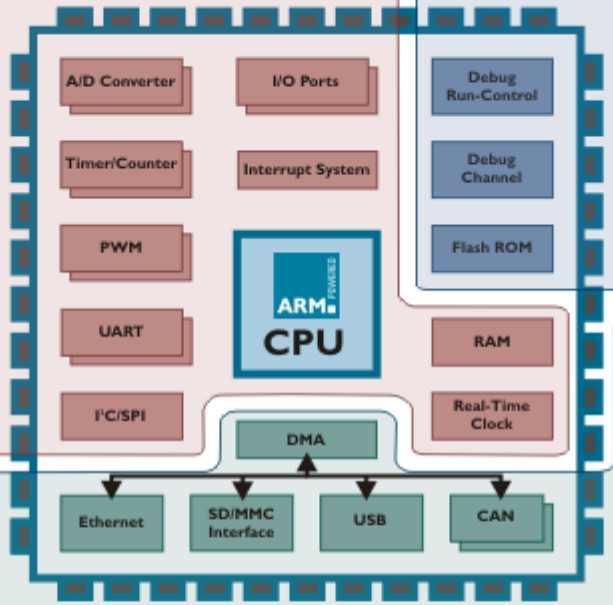
New Kinetis MCUs - Tool chain & 3rd Parties

Microcontroller Development Kit

CMSIS COMPLIANT

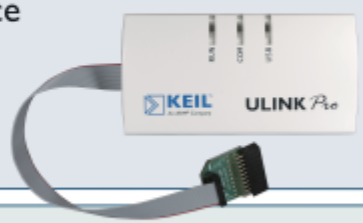
Complete software development environment for Cortex-M and ARM7/9 microcontrollers

Easy to learn and use, yet powerful enough for the most demanding embedded ARM application



ULINK USB Adapters

On-the-fly debugging and Flash programming via JTAG or serial interface



MDK-ARM
Microcontroller Development Kit

- ARM C/C++ Compiler
- Royalty-Free RTX RTOS
- µVision Device Database & IDE
- µVision Debugger & Analysis Tools
- Device Peripheral Simulation

Examples and Templates

RTX and Real-Time Library

Fully featured real-time kernel

Library of middleware components to speed up software development and solve real-time and communication challenges

RL-ARM
Real-Time Library

- RTX RTOS Source Code
- TCPnet Networking Suite
- Flash File System
- USB Device Interface
- CAN Interface

Examples and Templates

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New Kinetis MCUs - Tool chain & 3rd Parties

All tools & RTOSes owned, created and supported by Green Hills

World's largest ARM software tools supplier

Full Featured Real-Time Executive

- ✓ Ultra-small (2KB), fast, simple to use
- ✓ Royalty-free, includes source code
- ✓ TCP/IP v4/v6 networking suite
- ✓ Wear leveling Flash and MS/DOS file system
- ✓ USB device/mass storage class
- ✓ Embedded graphics library

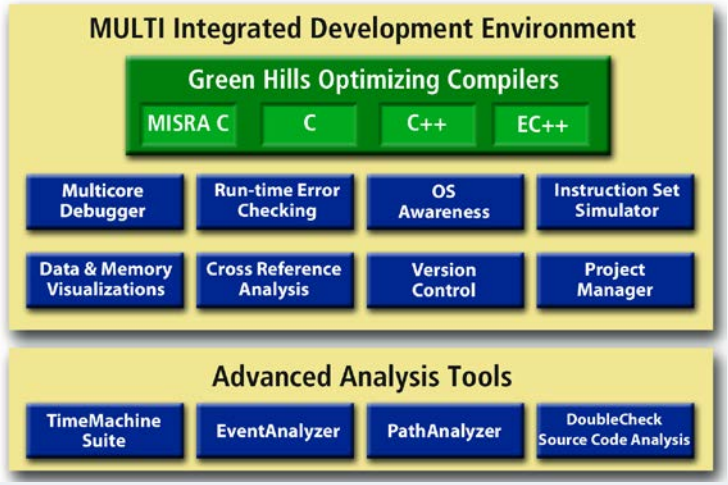
µ-velOSity

JTAG and Trace Hardware Probes

- ✓ Green Hills Probe – multiuser, high-speed debugging, download, flash programming via Ethernet or USB
- ✓ SuperTrace Probe – non-intrusive trace, download, and debugging via ARM Embedded Trace (ETM)

High quality, professional grade CMMI

Advanced Development Tools



Target markets

- ✓ Printers, barcode scanners
- ✓ Programmable logic controllers
- ✓ Smart meters, remote sensors
- ✓ Building automation, HVAC
- ✓ Heart rate monitors, Blood analyzers
- ✓ Instrumentation clusters
- ✓ Surveillance cameras

Free Full Featured 30-day Eval

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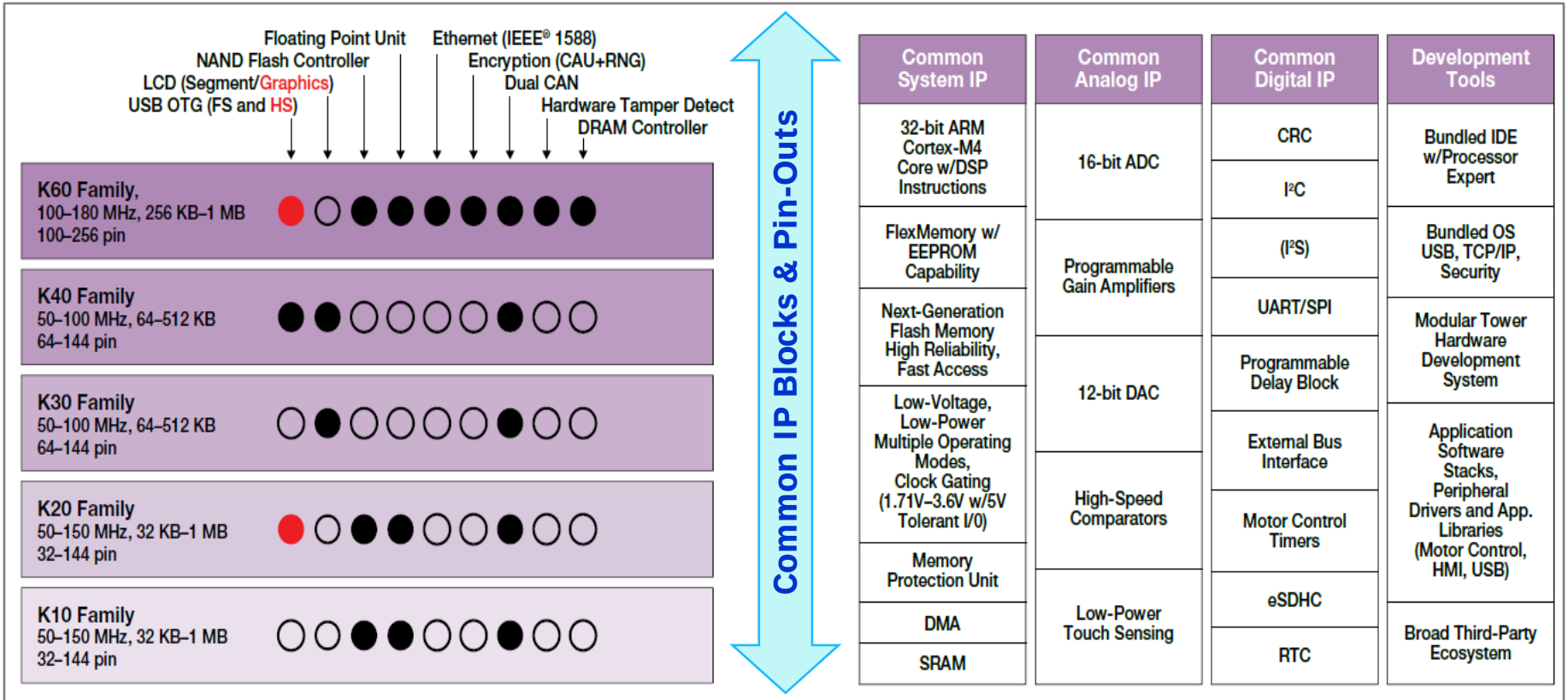
New Kinetis MCUs - Summery

ARM® Cortex™-M4 MCUs



Kinetis MCUs offer exceptional value with 10K starting prices from $0.99 for 32 KB flash memory devices in a 32-pin package.

The *first phase* of the portfolio consists of five MCU families with over 200 pin-, peripheral- and software compatible devices with outstanding performance, memory and feature scalability.

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Freescale ColdFire+ and Kinetis - Links

ColdFire+		http://www.freescale.com/webapp/sps/site/homepage.jsp?code=CFPLUS
Kinetis	K10....K70	http://www.freescale.com/Kinetis
	i.e. K60 Product Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=K60&tid=mKhp
	K60 Documentation	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=K60&fpsp=1&tab=Documentation_Tab
	K60 Product Brief	http://cache.freescale.com/files/32bit/doc/prod_brief/K60PB.pdf?fpsp=1&WT_TYPE=Product Briefs&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation
	K60 Reference Manual	http://cache.freescale.com/files/32bit/doc/ref_manual/K60P144M100SF2RM.pdf?fpsp=1&WT_TYPE=Reference Manuals&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation
	K60 DataSheet	http://cache.freescale.com/files/microcontrollers/doc/data_sheet/K60P144M100SF2.pdf?fpsp=1&WT_TYPE=Data Sheets&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation
	K60 ErrataSheet	http://cache.freescale.com/files/microcontrollers/doc/errata/KINETIS_0M33Z.pdf?fpsp=1&WT_TYPE=Errata&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation
MQX RTOS	Free RTOS	http://www.freescale.com/MQX *http://www.embedded-access.com*
eGUI	Free GUI Driver	*www.freescale.com/eGUI*
TowerKit	DemoBoard	http://www.freescale.com/Tower
Ecosystem	CodeWarrior (Eclipse)	http://www.freescale.com/CodeWarrior
	IAR EWARM	http://www.iar.com
	MDK-KEIL	http://www.keil.com
	CodeSourcery	http://www.codesourcery.com/
	Segger JLink	http://www.segger.com/cms

... and more.

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www.freescale.com/productlongevity

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Freescale has a longstanding track record of providing long-term production support for our products

Freescale offers a formal product longevity program for the market segments we serve

- For the automotive and medical segments, Freescale will make a broad range of program devices available for a minimum of 15 years
- For all other market segments in which Freescale participates, Freescale will make a broad range of devices available for a minimum of 10 years
- Life cycles begin at the time of launch

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Freescale Kinetis

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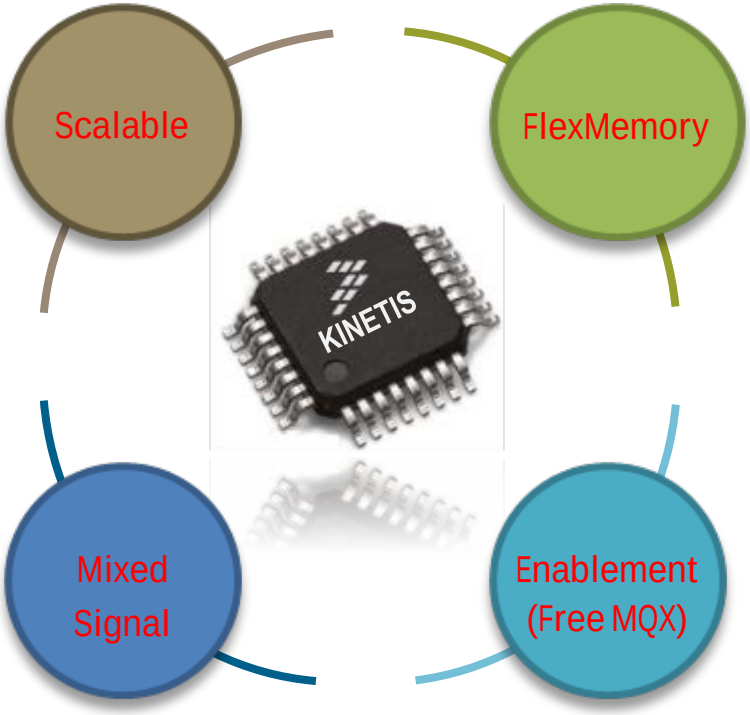

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