Rev 1.2

TECHNICAL DESCRIPTION

Fastrax IT500 GPS Receiver

This document describes the electrical connectivity and main functionality of the IT500 hardware.

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Fastrax Ltd.

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CHANGE LOG

Rev.	Notes	Date
1.0	Initial revision.	2009-06-01
1.01	Orientation of figure 3 corrected.	2009-06-17
1.1	- Maximum Vdd corrected to +4.2V. - Minimum application schematics updated. - Standby mode description added in chapter 3 - Explanation of FIX_VALID signal added as chapter 4.10.	2009-08-31
1.11	Support for UART protocol change by NMEA command removed from document (ch. 4.7).	2009-11-24
1.2	IT500U variant removed.	2010-11-02

CONTENTS

COMPLEMENTARY READING

The following Fastrax reference documents are complementary reading for this document. All operating and firmware related documentation is also available at ***www.fastraxgps.com***

Ref. #	Document name
1	IT MP Application Note
2	Fastrax 500 Series NMEA protocol specification
3	Module Soldering Profile

1. INTRODUCTION

The Fastrax IT500 is a GPS module, which provides receiver functionality using the low power, ultra-high performance MediaTek MT3329 chip. The module has compact form factor 16.2mm x 18.8mm, height is 2.3mm nominal (2.5mm max). The IT500 receiver provides low power operation and very fast TTFF. Extreme weak signal acquisition and tracking capability meet the most demanding performance expectations and enable even indoor operation. The receiver complies with the IT MultiPlatform (MP) connectivity and size, i.e. it is pin compatible with IT300 and IT03-S.

The Fastrax IT500 module provides complete signal processing from antenna to serial NMEA data output [2]. MTK Binary protocol can be used to push predicted ephemeris data into the IT500 receiver in AGPS applications.

The Fastrax IT500 module requires a power supply VDD, a backup supply voltage VDD_B for non-volatile RAM & RTC blocks, and GPS antenna input signal. The IT500 module interfaces to the customer's application via two serial ports, PPS timing signal, Fix valid indicator signal and active antenna detector status signals (2 outputs). Serial data and all I/O signal levels are CMOS compatible.

Optionally, there is a 32.768 kHz RTC output (1.2V CMOS level) available for customer application processor. A STANDBY control input (option) can be used to set the module in standby state while keeping the VDD supply active.

The antenna input supports passive and active antennas and provides also an internally generated and current limited antenna bias supply.

This document describes the electrical connectivity and main functionality of the IT500 module.

1.1. Default firmware configuration

Fastrax IT500 default firmware configuration:

1. Port 0: NMEA 9600 baud
2. Port 1: RTCM input, 9600 baud
3. NMEA output: GGA, RMC, GSV, GSA (all 1 sec interval)
4. DGPS/SBAS: Disabled, WAAS/EGNOS/MSAS can be enabled with NMEA command [2].
5. Datum: WGS84

2. SPECIFICATIONS

2.1. General

Table 1. General Specifications for IT500.

Receiver	GPS L1 C/A-code, SPS
Channels	22 tracking / 66 acquisition
Update rate	1 Hz default (fix rate configurable up to 10Hz)
Supply voltage, VDD	+3.0V…+4.2 V
Back up supply voltage, VDD_B	+2.0V…+4.2 V (preferably active all the time)
Power consumption, VDD	75 mW typical @ 3.0V (without Antenna bias)
Power consumption, VDD_B	15 uW typical @ 3.0V (during Back up state)
Power consumption, Standby mode	3mW typical @ 3.0V
Antenna net gain range	0…+25dB (including cable loss)
Antenna bias voltage	Same as VDD
Antenna bias current	3mA…30mA (internally limited to 40 mA)
Storage temperature	-40ºC…+85ºC
Operating temperature	-40ºC…+85ºC
Serial port configuration (default)	Port 0: NMEA; Port 1: RTCM
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed (default)	NMEA: 9600 baud
I/O signal levels	CMOS 2.8V compatible: low state 0.0…0.3xVDD; high state 0.7…1.0xVDD. Note: FOUT_32K is 1.2V CMOS compatible.
I/O sink/source capability	+/- 2 mA max. (20uA for XANTSHORT)
PPS output	+/- 50ns accuracy

2.2. Absolute maximum ratings

Table 2. Absolute maximum ratings.

Item	Min	Max	Unit
Operating and storage temperature	-40	+85	ºC
Power dissipation	-	500	mW
Supply voltage, VDD	-0.3	+4.2	V
Supply voltage, VDD_B	-0.3	+4.2	V
Supply voltage, VDD_USB	-0.3	+6.0	V
Current output on antenna input	0	+50	mA
Input voltage on any input connection	-0.3	VDD + 0.3	V
RF input level	-	+15	dBm

3. OPERATION

3.1. Operating modes

After power up the receiver boots from the internal flash memory for normal operation. Modes of operation:

- Tracking/navigating mode
- Low power tracking/navigating mode
- Standby mode
- Backup mode

3.2. Tracking/Navigating mode

In tracking/navigating mode the Fastrax IT500 receiver module will search for satellites and collects almanac data. Once the receiver has collected almanac data (this takes about 12 minutes from Factory Cold Start) and stored it in internal Flash memory, it will automatically enter Low Power Tracking mode. The VDD power consumption in table 1 is measured in Low Power Tracking/Navigating mode.

3.3. Low Power Tracking/Navigating mode

In Low power tracking/navigating mode the receiver continues normal navigation but does not collect further Almanacs data (ephemeris data is collected whenever new satellites become visible). Therefore the current consumption is reduced to level of <75 mW.

3.4. Standby mode

In Standby mode the IT500 receiver is shutting down the RF-part (including antenna bias) of the module and puts the processor in standby mode. RTC oscillator is running and RAM content is maintained over the Standby period. The current consumption is greatly reduced from Low Power Tracking/Navigating mode, but remains higher than in Backup mode (see table 1). The Standby mode is initiated by falling edge at STANDBY pin. The module can be wake up from Standby mode by rising edge at the STANDBY pin.

3.5. Backup mode

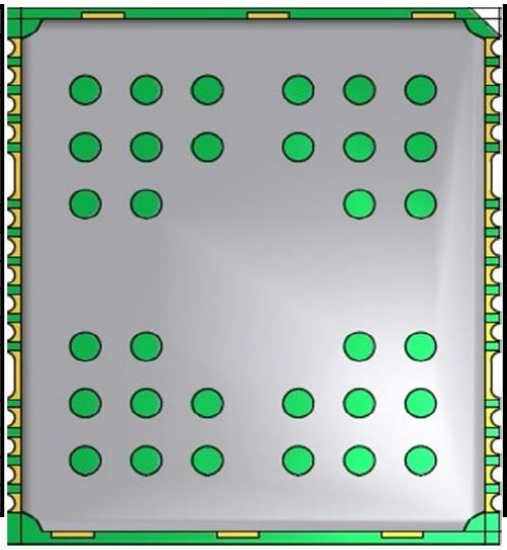
When the operating voltage VDD is removed from the Fastrax IT500, the module enters Backup mode. In this mode, the module is keeping time by the RTC oscillator. Also, satellite ephemeris data is stored in battery backup RAM in order to get fast TTFF when VDD is reconnected. Any user configuration settings are also valid as long as the backup supply BU is active. When the BU is powered off, the configuration is reset to factory configuration on next power up.

It is possible to connect an external backup battery to dedicated pin on the Fastrax IT500. In this case, both supply voltages may be disconnected and the external backup battery will keep RTC and RAM supply active enabling fast recovery once the supply voltages are switched on again.

3.6. Pin states in different modes

The picture below will present the IO pin states of the IT500 module in different operating modes.

Pin Name	RST	OP	STB	Pin
No Connect	nc	nc	nc	1
No Connect	nc	nc	nc	2
No Connect	nc	nc	nc	3
No Connect	nc	nc	nc	4
GND	gnd	gnd	gnd	5
No Connect	nc	nc	nc	6
BU_BATT	1.2	1.2	1.2	7
STANDBY	PU	PU	0	8
XRESET	0	PU	PU	9
No Connect	nc	nc	nc	10
GND	gnd	gnd	gnd	11
FOUT_32K	0	0	0	12
FIX_VALID	0	Fix	2.8	13
VDD_B	VB	VB	VB	14
GND	gnd	gnd	gnd	15



Pin	STB	OP	RST	Pin Name
30	0	pps	0	PPS
29	nc	nc	nc	No Connect
28	V	V	V	VDD
27	0	0	H	ANT_OK 1)
26	gnd	gnd	gnd	GND
25	gnd	gnd	gnd	GND
24	0	V	0	RF_IN
23	gnd	gnd	gnd	GND
22	gnd	gnd	gnd	GND
21	0	V	0	XANTSHORT
20	gnd	gnd	gnd	GND
19	3.3	3.3	3.3	RXD1 2)
18	3.3	3.3	3.3	RXD0 2)
17	H	tx	H	TXD0
16	H	tx	H	TXD1

OP = Normal Operation
RST = Reset State
STB = Standby State

PU = Pull-up input (2.8V)
Fix = Valid fix function output.
tx = UART tx data (NMEA)

H = CMOS output, High (2.8V)
V = VDD, VB = VDD_B

Note 1) Passive antenna assumed. With active antenna ANT_OK = H in OP mode.
Note 2) Externally pulled up to 3.3V in Fastrax ev-kit. Customer pull-up voltage may be lower (e.g. 3.0V).

Figure 1. IT500 IO pin states in different operating states.

4. CONNECTIVITY

4.1. Connection assignments

The I/O connections are available as soldering pads on the bottom side of the module. These pads are also used to attach the module on the motherboard in application. All unconnected I/O should be left open (floating).

Table 3. IT500 Module Connections.

Contact	Signal name	I/O	Alternative signal name	Signal description
1	n.c.	-	-	Not connected
2	n.c.	-	-	Not connected
3	n.c.	-	-	Not connected
4	n.c.	-	-	Not connected
5	GND	-	-	Ground
6	n.c.	-	-	Not connected
7	BU_BATT	-	-	External backup battery of Super capacitor. Leave open if not used.
8	STANDBY	I	-	Standby mode (see note 1). Leave open if not used.
9	XRESET	I	-	Asynchronous system reset, active when low.
10	NC	-	-	Not connected
11	GND	-	-	Ground
12	n.c.	O	FOUT_32K	FOUT_32K function is an option and has to be requested from Fastrax.
13	FIX_VALID	O	-	Valid fix indicator.
14	VDD_B	I	-	Power supply for battery back up
15	GND	-	-	Ground
16	TXD1	O	-	UART 1 async. output
17	TXD0	O	-	UART 0 async. output

18	RXD0	I	-	UART 0 async. input
19	RXD1	I	-	UART 1 async. input
20	GND	-	-	Ground
21	XANTSHORT	O	-	Antenna short circuit indicator. Normally high. Low when antenna input is shorted to GND.
22	GND	-	-	Ground
23	GND	-	-	Ground
24	RFIN	I/O	-	Antenna signal input, Antenna bias voltage output.
25	GND	-	-	Ground
26	GND	-	-	Ground
27	ANT_OK	O	-	Active antenna status indicator.
28	VDD	I	-	Main Power supply.
29	n.c.	-	-	Not connected
30	PPS	O	-	1PPS signal output
Contact	**Signal name**	**I/O**	**Alternative GPIO name**	**Signal description**

4.2. Power supply

The Fastrax IT500 module requires two separate power supplies: VDD_B for non-volatile back up block (RTC/RAM) and the VDD for digital parts and I/O. RF block has internally regulated +2.8V supply. VDD can be switched off when navigation is not needed but if possible keep the backup supply VDD_B active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF. Note that VDD_B can also be switched off and backup functionality still maintained if an external backup battery is connected to module pin #7 (see Chapter 6.1).

Back up supply VDD_B draws typically 5 uA current in back up state. During navigation VDD_B current typically peaks up to 55 uA and is in average 30-40 uA.

Main power supply VDD current varies according to the processor load and satellite acquisition. Maximum VDD peak current is about 40 mA during acquisition.

NOTE

Backup supply VDD_B has to be connected whenever VDD is connected.

4.3. Reset

The reset input XRESET is an active low asynchronous reset. The processor boots after the low-to-high transition. At power down the reset is forced when the VDD drops below 2.8 V. For normal operation the XRESET input can be left unconnected.

4.4. STANDBY control input

Fastrax IT500 has a standby pin. Firmware support for standby will be introduced in Q4/2009.

NOTE

If not used, leave STANDBY not connected (nc).

4.5. Antenna input

The module supports passive and active antennas. The antenna input impedance is 50 ohms. During normal (navigating) operation, the input provides also a bias supply (the same as VDD). When the navigation is stopped (e.g. VDD removed or XRESET pulled low), the antenna bias is switched off internally.

There is an internal current limiter for the active antenna bias of about 40mA on the Fastrax IT500 module. If more current is drawn (for example in case of antenna short circuit) the fault is indicated by antenna status output bits. Also, if the active antenna is removed (or antenna cable is cut), the state is indicated by the antenna status bits. The antenna status indicator bit states are described in table below.

Table 4. Active antenna status output signals.

GPIO	Active Antenna OK	Antenna short	Antenna open or passive antenna
ANT_OK	High	Low	Low
XANTSHORT	High	Low	High

NOTE

Passive antennas with a short-circuit to GND should be DC blocked externally with a 18pF…1nF serial capacitor.

NOTE

With passive antenna keep the cable loss at minimum (<1dB).

4.6. Active GPS antenna

The customer may use an external active GPS antenna for e.g. in mobile or indoor usage. It is suggested the active antenna has a net gain *including cable loss* in the range 0 dB…+25 dB.

4.7. UART

The device supports UART communication via Port 0 and Port 1. With the standard firmware the Port 0 is configured by default to NMEA protocol with 9600 baud and Port 1 to RTCM protocol (input) with 9600 baud.

The default configuration for Ports can be changed by commands via NMEA [2]. Any custom configuration stays active as long as the backup supply VDD_B is active.

I/O levels form the serial ports are CMOS compatible, not RS232 compatible. Use an external level converter to provide RS232 levels when needed.

4.8. PPS

The pulse-per-second (PPS) output provides an output for timing purposes. There is a 100ms pulse once per second when the receiver has a valid position fix available.

4.9. FIX_VALID

FIX_VALID signal indicates if there is a valid GPS fix available. When there is no valid fix available, this signal is at constant low state (‘0’). When a valid fix is available, this signal is toggling between low and high state at 0.5Hz and 50% duty cycle (1sec high, 1sec low).

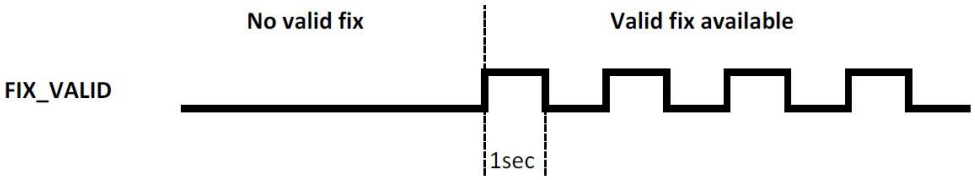


Figure 2. FIX_VALID output operation.

4.10. Mechanical dimensions and contact numbering

Module size is 16.2mm (typ.) x 18.8mm (typ.) x 2.3mm (typ). General tolerance is ±0.2mm.

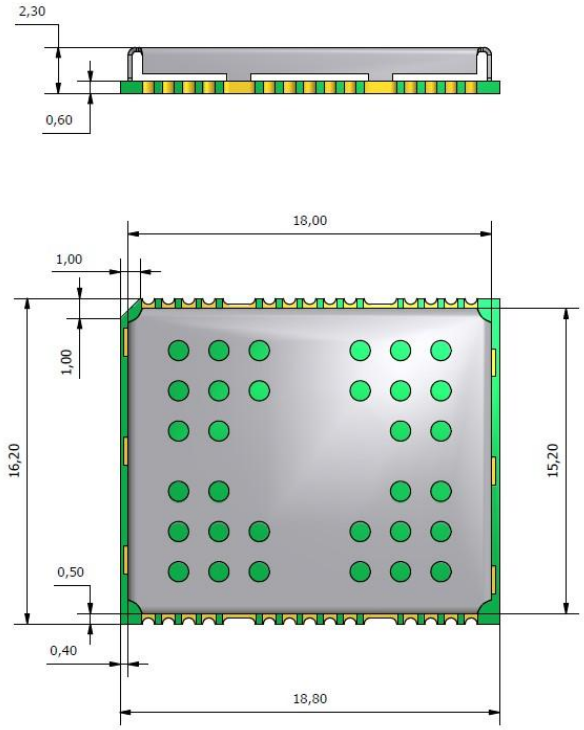


Figure 3. IT500 nominal dimensions (all dimensions in mm).

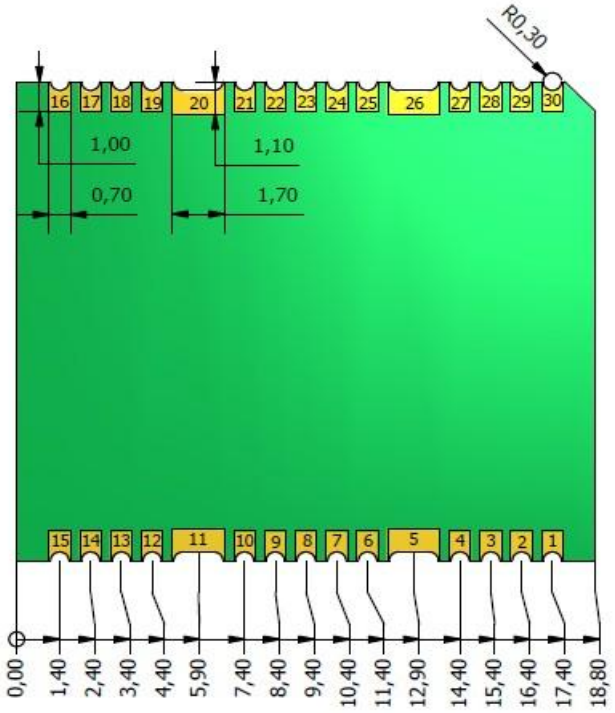


Figure 4. IT500 contact numbering (Bottom View).

4.11. Suggested pad layout

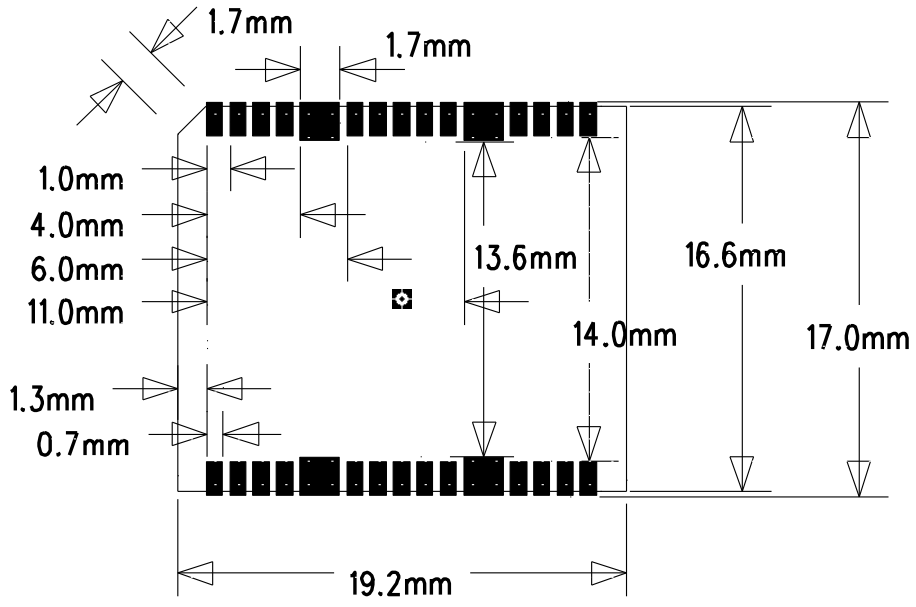


Figure 5. Suggested pad layout and occupied area (Top View).

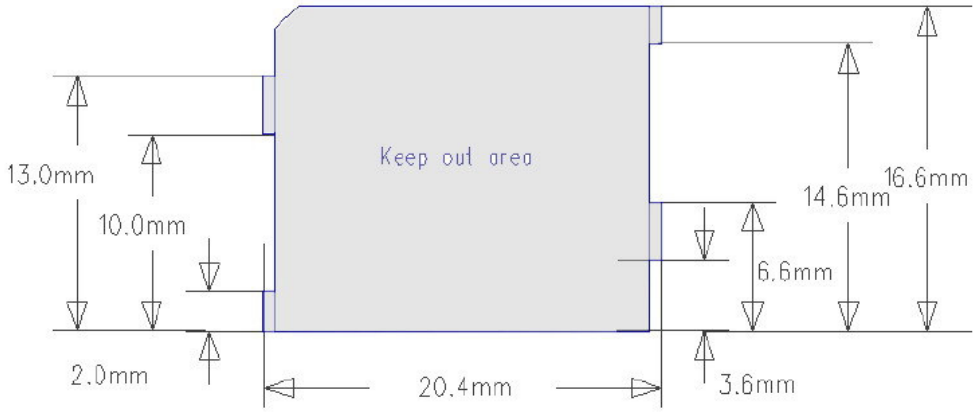


Figure 6. Suggested component keep out area (Top View).

5. MANUFACTURING

5.1. Assembly

The IT500 module supports only assembly and soldering in a reflow process on the top side of the PCB. Application note [3] will describe this in more detail.

5.2. Moisture sensitivity

Note that the IT500 is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

5.3. Tape and reel

One reel contains 500 modules. Reel specification is shown in Figure 5.

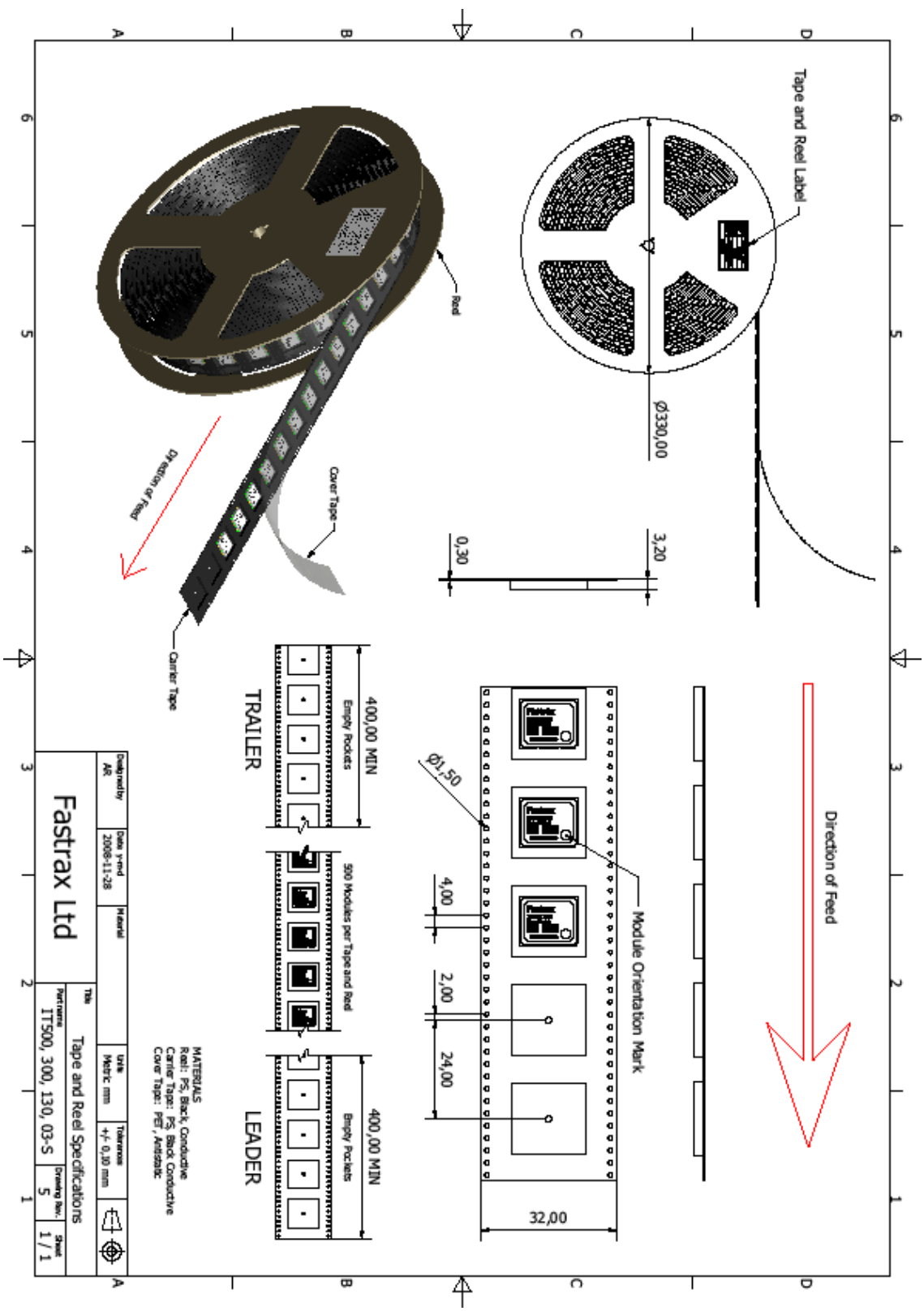


Figure 7. Reel specification.

6. REFERENCE DESIGN

The reference design gives a guideline for the applications using the IT500 GPS module. In itself it is not a finished product, but an example that performs correctly. There is an application note [1] available for further details on design for the IT MP family modules.

In the following two chapters the reader is exposed to design rules that should be followed, when designing an IT500 in to the application. By following the rules an optimal design with no unexpected behavior caused by the PCB layout itself can be created. These guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques and high speed logic.

6.1. Minimum Application Circuit Diagram

The Minimum Application supports communication through the UART Port 0 (NMEA protocol). Other required signals are the antenna input, supply voltage for VDD and VDD_B, and GND.

The low drop-out linear regulator (LDO) U1 supplies +3.0 V to VDD. The super capacitor C6 provides backup supply to VDD_B. The backup supply can be provided also from a coin cell battery or from any available back up supply with suitable voltage range.

All digital signals are routed away from the module through series resistors (R1…R6). In this way the local oscillator (LO) signal leakage that is present in the I/O contacts of the GPS module is suppressed. Although the LO leakage is very small at the IO contacts of the module, it may still interfere the GPS reception, especially when the antenna is located very near to these signal routes. Place these series resistors close to the module with short traces.

For the same reason capacitors C4 and C5 should be connected very close to the module with short traces to I/O contacts and to ground plane.

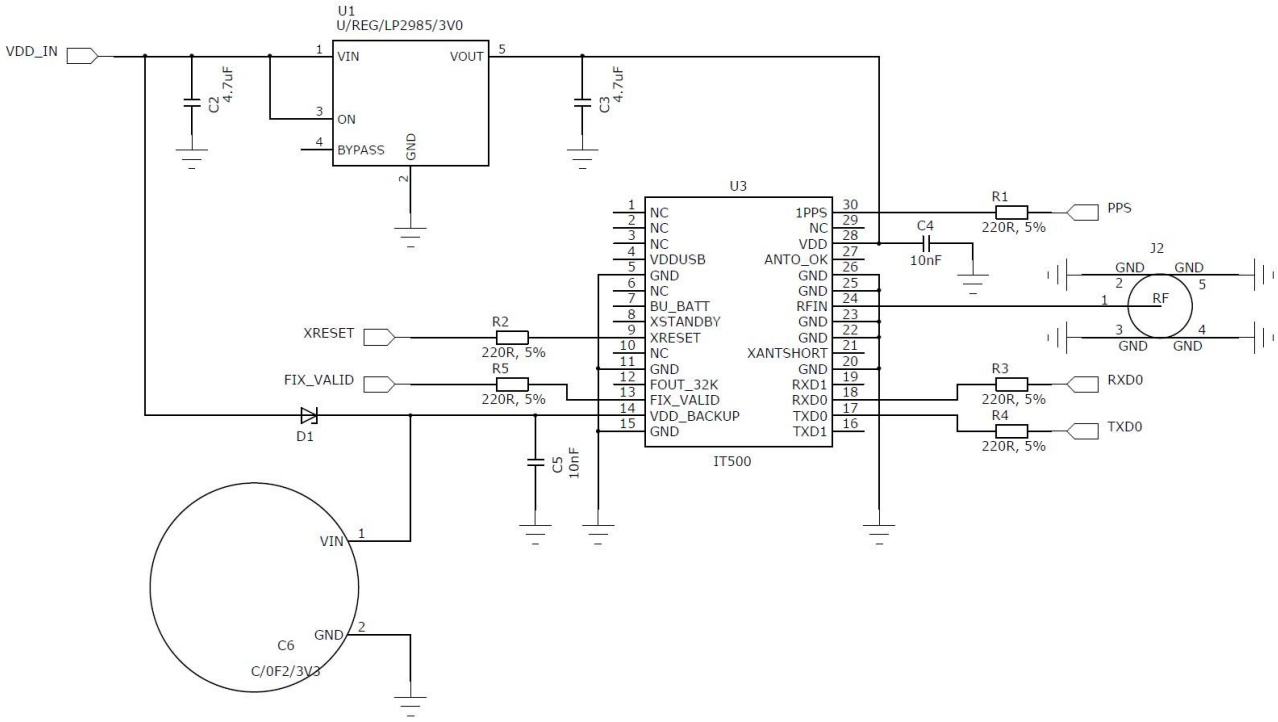


Figure 8. Minimum Application Circuit Diagram with IT-MP compatible VDD_BACKUP connectivity.

The application circuit can be further simplified, and one diode removed, by connecting the backup super capacitor on the BU_BATT pin of the IT500. However, this connectivity is not IT-MP compatible for super capacitor section of the design. If the super capacitor is left out, also this circuit can be used with other IT-MP modules but without backup functionality.

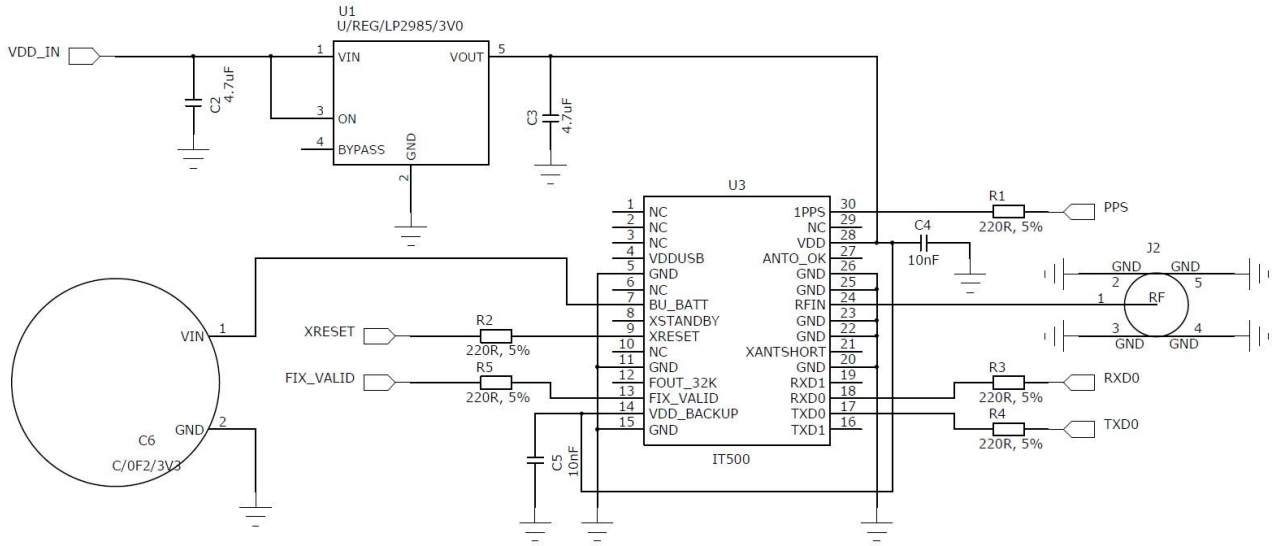


Figure 9. Minimum application circuit diagram, IT500 specific backup super capacitor connection.

Note that there is a DC bias voltage present at the RF input, when the module is operating in Navigating mode. If a passive antenna with short-circuit to GND is used, an external series DC block capacitor (18pF…1nF) must be used for the RFIN signal line.

6.2. PCB layout issues

The suggested 4-layer PCB build up is presented in the following table.

Table 5. Suggested PCB build up.

Layer	Description
1	Signal + Ground with copper keep-out below IT500
2	Ground plane
3	Signal + Ground or VDD plane
4	Signal (short traces) + Ground

Routing signals on top layer directly under the module should be avoided. This area should be dedicated to keep-out to both traces and to ground (copper), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be also minimized.

For a multi-layer PCB the first inner layer below the IT500 is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should placed very near to the IT500 module. In this way the risk for the local oscillator leakage is minimized. For the same reason by-pass capacitors C4 and C5 should be connected very close to the module with short traces to IO contacts and to the ground plane. Place the GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the IT500 to ground plane with short traces to via holes, which are connected to the ground plane. Use preferably two via holes for each GND pad.

The RF input should be routed clearly away from other signals. This minimizes the possibility of interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate and on the height between the signal trace and the first ground

plane. With FR-4 material the width of the trace shall be two times the substrate height.

A board space free of any traces should be covered with copper areas (GND). In this way, a solid RF ground is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures.

7. IT500 APPLICATION BOARD

The IT500 Application Board provides the IT500 connectivity to the IT Evaluation Kit, IT Mini Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the IT500 module, one regulator for VDD supply, a 0.2F super capacitor for VDD_B back up supply, an MCX antenna connector and a 2x20 pin Card Terminal connector.

7.1. Card Terminal I/O-connector

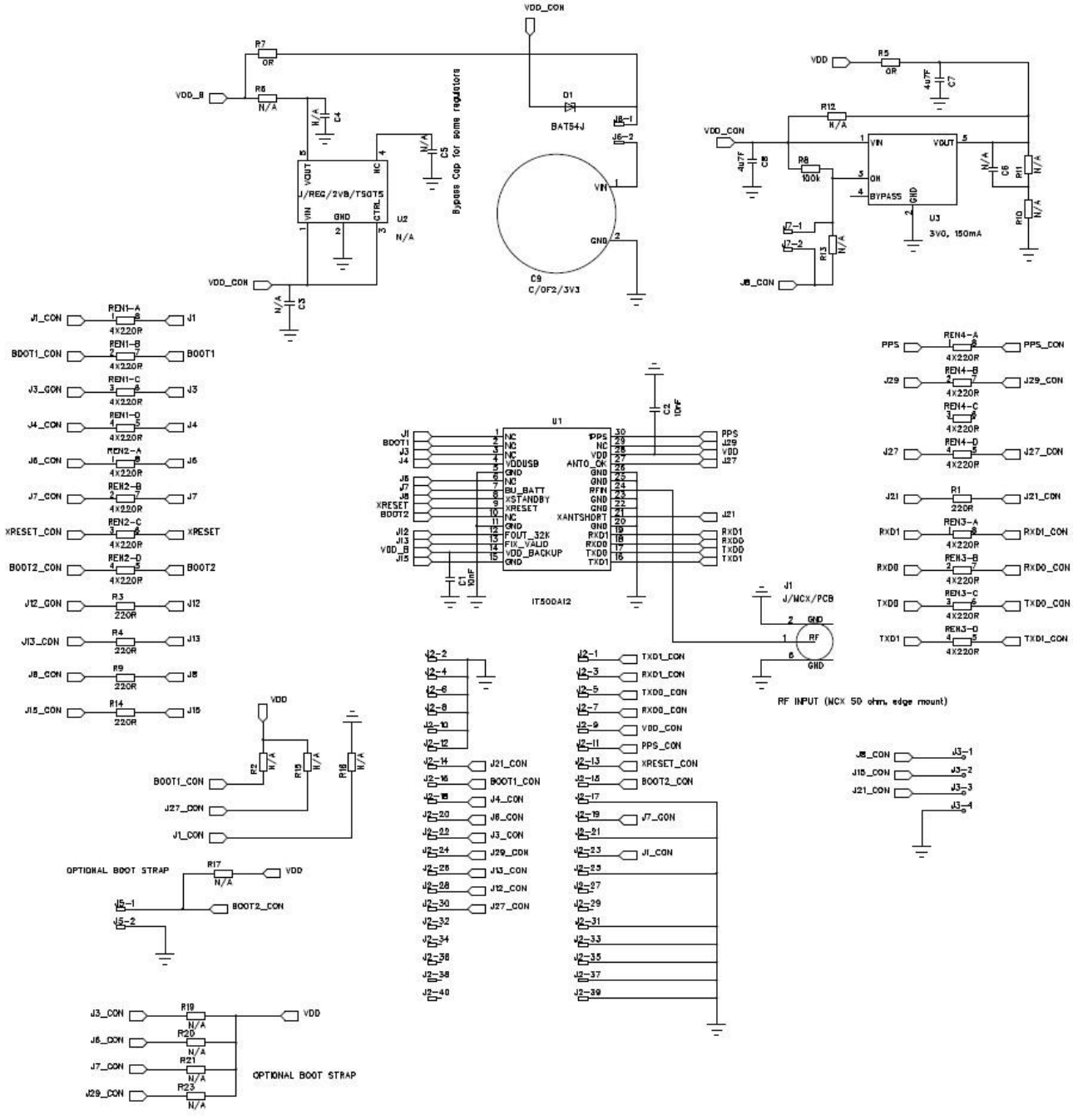
The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the IT Evaluation Kit pin header J4. Note that serial Port A and B maps to Port 0 and 1 at the Evaluation Kit, respectively.

Table 6. IT500 Application Board connectivity.

Pin #	Signal name	I/O	Alternative GPIO name	Interface to IT Evaluation Kit
1	TXDB	O	-	UART 1 async. output
2	GND	-	-	Ground
3	RXDB	I	-	UART 1 async. input
4	GND	-	-	Ground
5	TXDA	O	-	UART 0 async. output
6	GND	-	-	Ground
7	RXDA	I	-	UART 0 async. input
8	GND	-	-	Ground
9	VDD	P	-	Power input +3.3V
10	GND	-	-	Ground
11	PPS	O	-	1PPS signal output
12	GND	-	-	Ground
13	XRESET	I	-	Active low async. system reset
14	XANTSHORT	O	-	Not connected
15	-	-	-	Not connected
16	-	-	-	Not connected
17	GND	-	-	Ground
18	VDD_USB	P	-	Led Indicator D7
19	BU_BATT	P	-	Led Indicator D4

20	-	-	-	Led Indicator D6
21	GND	-	-	Ground
22	-	-	-	Led Indicator D5
23	-	-	-	Led Indicator D3
24	-	-	-	Led Indicator D2
25	GND	-	-	Ground
26	FIX_VALID	O	-	User Interface Indicator UI_ B
27	-	-	-	Not connected
28	FOUT_32K	O	-	Led Indicator D8
29	-	-		Not connected
30	ANTOK	O	-	User Interface Indicator UI_A
31	GND	-	-	Ground
32	-	-	-	Not connected
33	GND	-	-	Ground
34	-	-	-	Not connected
35	GND	-	-	Ground
36	-	-	-	Not connected
37	GND	-	-	Ground
38	-	-	-	Not connected
39	GND	-	-	Ground
40	-	-	-	Not connected
Pin #	**Signal name**	**I/O**	**Alternative GPIO name**	**Interface to IT Evaluation Kit**

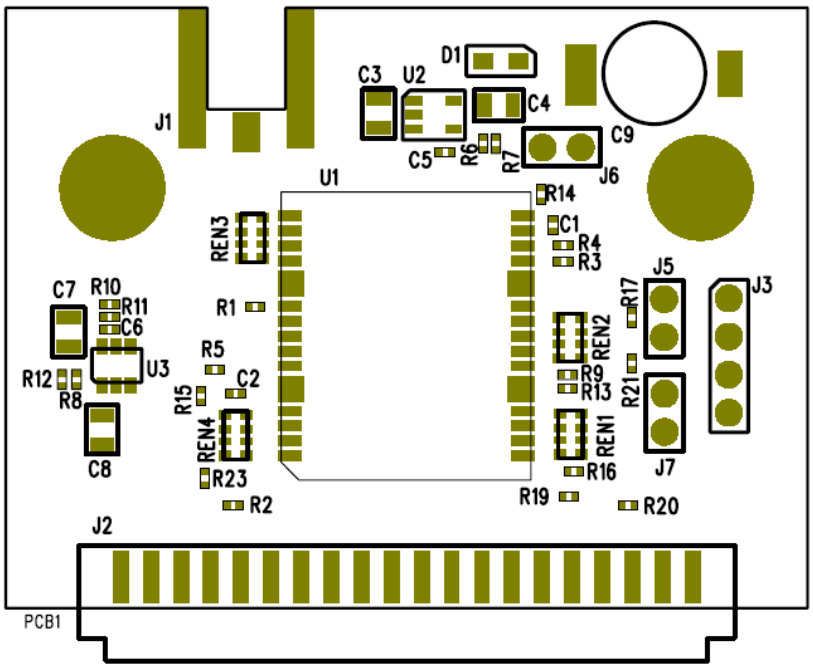
7.2. Circuit Diagram



7.3. Bill of materials

Qty	Reference	TECHNICALDESCRIPTION
1	C1	10nF 16V 10% X7R 0402
1	C2	10nF 50V 10% X7R 0402
2	C7-8	4,7uF 6,3V X5R 0805 +20%
1	C9	CAP BACKUP 3V3 / 0F2
1	D1	Diode 75V 225mA, BAT54J
2	H3-4	FIDUCIAL, Circle, rectangle, triangle
2	H1-2	Hole 3.0mm
1	U1	IT500
1	J6	1x2 pin-header, straight, 2,54mm
1	J2	EDGE MOUNT SOCKET STRIP 40 PINS
1	J1	50 Ohm male MCX connector PCB
1	PCB1	Application board for PCB IT MP, Rev. A
2	R5 R7	0R 0402
1	R8	100k 5% 0402 63mW
5	R1 R3-4 R9 R14	220R 5% 0402 63mW
4	REN1-4	4 x 220R ARV241
1	S1	Jumper, Pitch, 2.54mm, Red colour
1	U3	Reg. 3V0, 150mA

7.4. Assembly drawing, Top side



7.5. Artwork

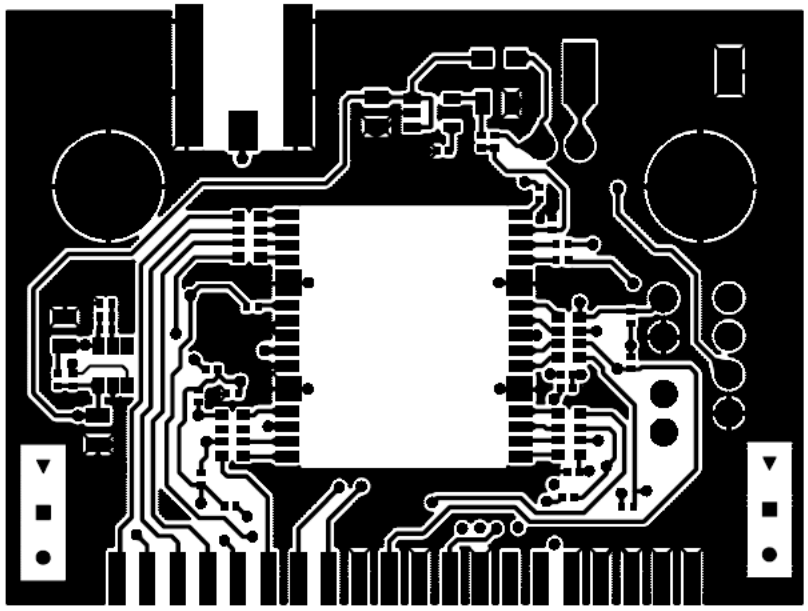


Figure 10. Layer 1 (top).

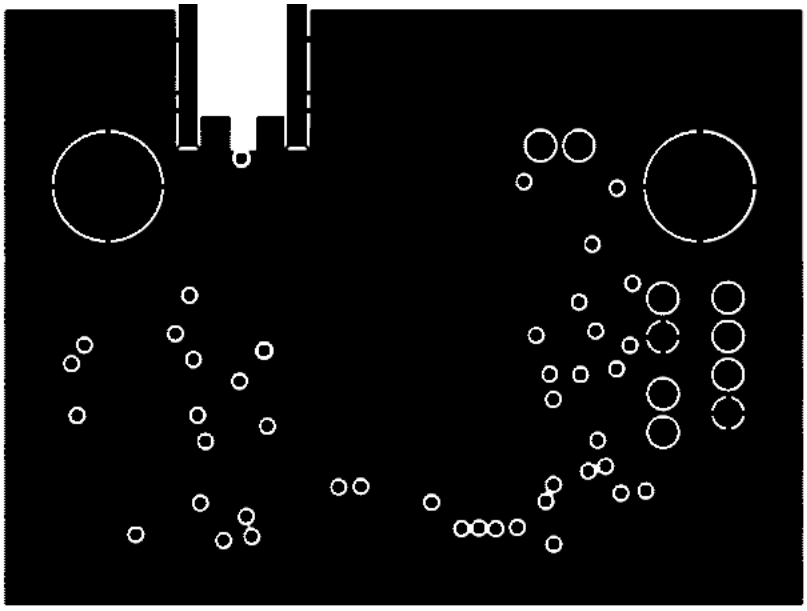


Figure 11. Layer 2.

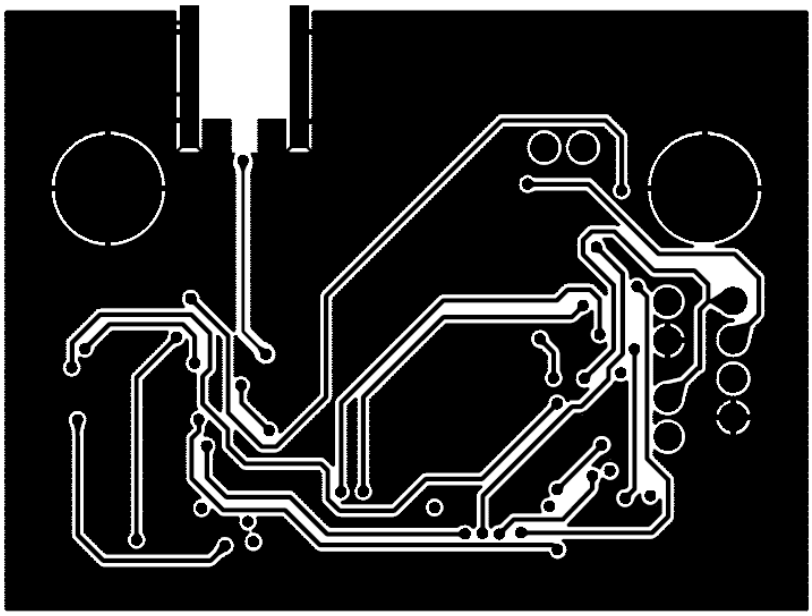


Figure 12. Layer 3.

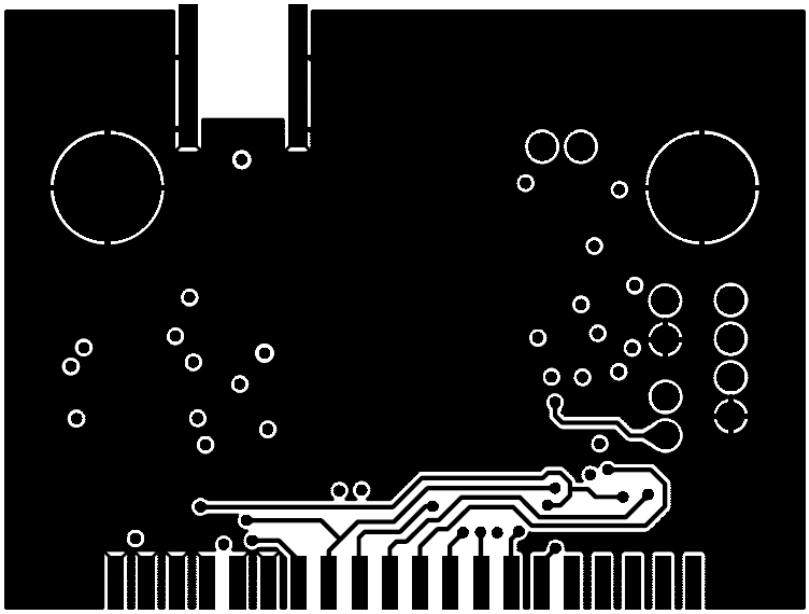


Figure 13. Layer 4.

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