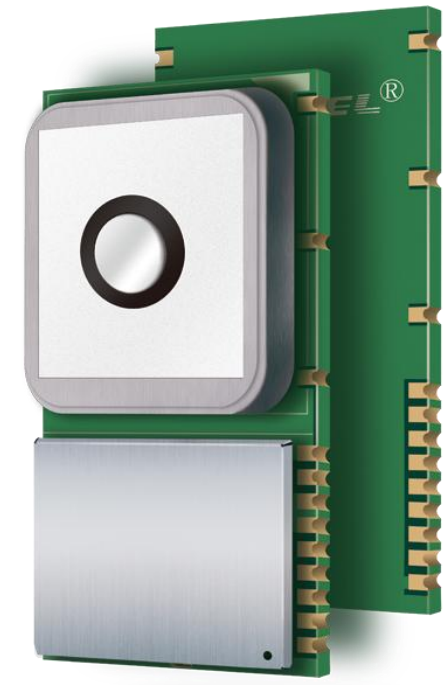
L50

Quectel GPS Engine



Hardware Design

L50_HD_V1.0

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0. Revision History

Revision	Date	Author	Description of change
1.0	2011-07-25	Baly BAO/Harry LIU	Initial

1. Introduction

This document defines and specifies L50 GPS module. It describes L50 hardware interface and its external application reference circuits, mechanical size and air interface.

This document can help customer quickly understand module interface specifications, electrical and mechanical characteristics. With the help of this document and other application notes, customers can use L50 module to design and set up application quickly.

1.1 Related Documents

Table 1: Related documents

SN	Document name	Remark
[1]	L50_EVB _UGD	L50 EVB User Guide
[2]	L50_GPS_Protocol	L50 GPS Protocol Specification
[3]	SIRF_AGPS_AN	SIRF Platform A-GPS Application Note

1.2 Terms and Abbreviations

Table 2: Terms and abbreviations

Abbreviation	Description
CGEE	Client Generated Extended Ephemeris
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
EGNOS	European Geostationary Navigation Overlay Service
GPS	Global Positioning System
GNSS	Global Navigation Satellite System
GGA	GPS Fix Data
GLL	Geographic Position – Latitude/Longitude
GSA	GNSS DOP and Active Satellites
GSV	GNSS Satellites in View
HDOP	Horizontal Dilution of Precision
IC	Integrated Circuit
I/O	Input/Output
Kbps	Kilo Bits Per Second
LNA	Low Noise Amplifier
MSAS	Multi-Functional Satellite Augmentation System
NMEA	National Marine Electronics Association

OSP	One Socket Protocol
PDOP	Position Dilution of Precision
RMC	Recommended Minimum Specific GNSS Data
SBAS	Satellite-based Augmentation System
SUPL	Secure User Plane Location
SAW	Surface Acoustic Wave
TBD	To Be Determined
TTFF	Time-To-First-Fix
UART	Universal Asynchronous Receiver & Transmitter
VDOP	Vertical Dilution of Precision
VTG	Course over Ground and Ground Speed, Horizontal Course and Horizontal Velocity
WAAS	Wide Area Augmentation System
ZDA	Time & Date
Inom	Nominal Current
Imax	Maximum Load Current
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value

2. Product Concept

L50 is a GPS ROM-based module with embedded GPS patch antenna and features fast acquisition and tracking with the latest SiRF Star IV technology. This module provides outstanding GPS performance in a slim package. Based on an external optional EEPROM which provides capability of storing ephemeris and downloading patch codes through UART, L50 can support Standalone and A-GPS (CGEE function). Advanced jamming suppression mechanism and innovative RF architecture, L50 provides a higher level of anti-jamming and ensures maximum GPS performance. The module supports location, navigation and industrial applications including autonomous GPS C/A, SBAS (WAAS or EGNOS) and A-GPS. Furthermore, a patch antenna has been designed into the L50 module. This will reduce customers' design complexity greatly.

- L50, in SMD type, can be embedded in customer applications via the 24-pin pads with the slim 16 x 28 x 3mm package. It provides all hardware interfaces between the module and host board.
- The multiplexed communication interface: UART/I2C/SPI interface.
- The Dead Reckoning I2C interface up to 400Kbps can be used to connect with an external EEPROM to save ephemeris data for CGEE function and to store patch codes.

The module is RoHS compliant to EU regulation.

2.1 Key Features

Table 3: Module key features

Feature	Implementation
Power supply	supply voltage: 1.71V – 1.89V typical : 1.8V
Power consumption	● Acquisition 45 mA @ -130dBm ● Tracking 35 mA @ -130dBm ● Hibernate 20uA
Receiver Type	● GPS L1 1575.42MHz C/A Code ● 48 search channels
Sensitivity[1]	● Cold Start (Autonomous) -148 dBm ● Reacquisition -160dBm ● Hot Start -160 dBm ● Tracking -163 dBm ● Navigation -160 dBm
Time-To-First-Fix[1]	● Cold Start (Autonomous) <33s ● Warm Start (Autonomous) <33s ● Warm Start (With CGEE) 10s typ. ● Hot Start (Autonomous) <1s
Horizontal Position Accuracy	● <2.5 m CEP
Max Update Rate	● 1Hz

Accuracy of 1PPS Signal	● Typical accuracy 61 ns ● Time pulse 200ms
Velocity Accuracy	● Without aid 0.01 m/s
Acceleration Accuracy	● Without aid 0.1 m/s ^{2}
Dynamic Performance	● Maximum altitude 18288m ● Maximum velocity 514m/s ● Acceleration 4 G
Dead Reckoning I2C Interface	● CGEE ● Open drain output ● MEMS support (TBD devices) ● Standard I2C bus maximum data rate 400kbps ● Minimum data rate 100kbps
Communication interface	● Support multiplexed UART/I2C interface ● The output is CMOS 1.8V compatible and the input is 3.6V tolerant
Temperature range	● Normal operation: -40 ℃ ~ +85 ℃ ● Storage temperature: -45 ℃ ~ +125 ℃
Physical Characteristics	Size: 16±0.15 mm x 28±0.15 mm x 3±0.2mm Weight: Approx. 4 g

Measured in conducted method by 8-star GPS simulator

2.2 Functional Diagram

The block diagram of L50 is shown in the Figure 1.

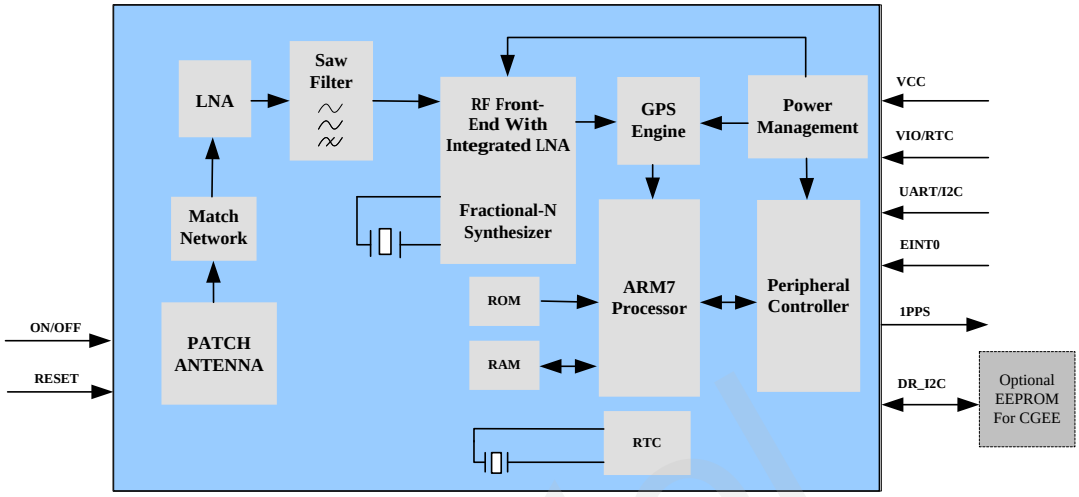


Figure 1: Functional diagram for L50

2.3 Evaluation Board

In order to help customers to develop applications with L50, Quectel offers an Evaluation Board (EVB) with appropriate power supply, RS-232 serial port and EEPROM.

Note: For more details, please refer to the document [1].

2.4 Protocol

L50 supports standard NMEA-0183 protocol and the One Socket Protocol (OSP), which is the binary protocol interface that enables customers' host device to access all SiRF GPS chip products of the SiRF Star IV family and beyond. The module is capable of supporting the following NMEA formats: ***GGA, GSA, GLL, GSV, RMC, and VTG***.

Table 4: The module supports protocols

Protocol	Type
NMEA	Input/output, ASCII, 0183, 3.01
OSP	Input/output, OSP protocol

Note: Please refer to document [2] about NMEA standard protocol and SiRF private protocol.

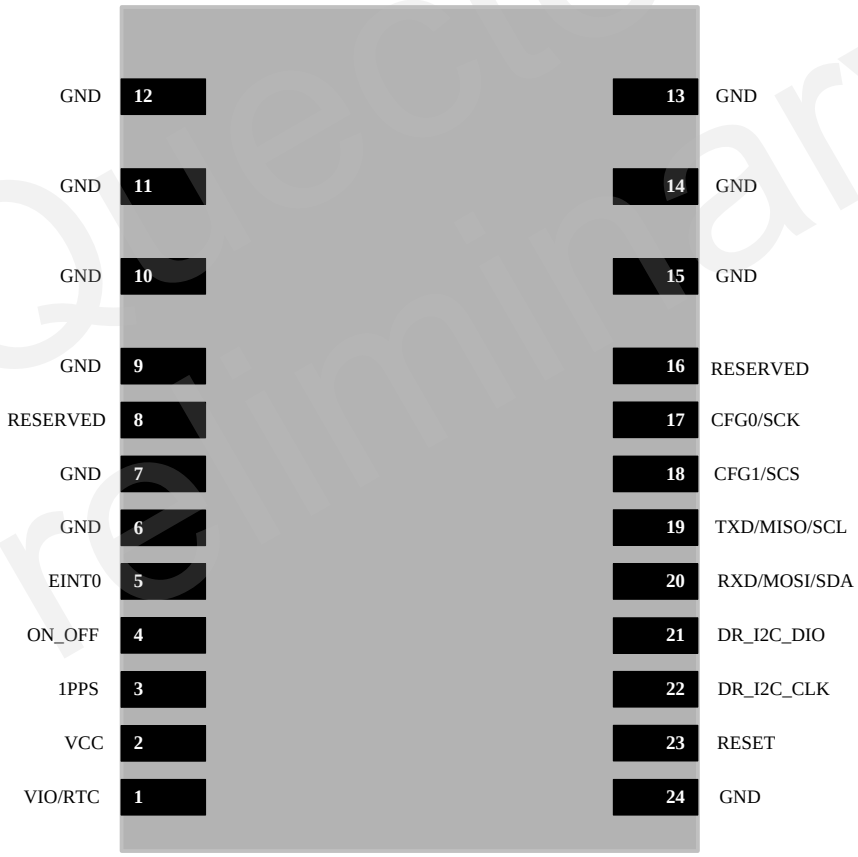
3. Application

L50 is a 24-pin surface mounted device (SMD) which could be embedded into customers' application conveniently. Sub-interfaces included in these pins are described in detail in the following chapters:

- Power management *(refer to Chapter 3.4)*
- Power supply *(refer to Chapter 3.5)*
- Timing sequence *(refer to Chapter 3.6)*
- Communication interface *(refer to Chapter 3.7)*
- Assisted GPS *(refer to Chapter 3.8)*

Electrical and mechanical characteristics of the SMD pad are specified in *Chapter 5 & Chapter 6.*

3.1 Pin Assignment of the Module



3.2 Pin Description

Table 5: Pin description

Power Supply					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
VCC	2	I	Supply voltage	Vmax= 1.89V Vmin=1.71V Vnom=1.8V	Supply current should be no less than 100mA.
VIO/RTC	1	I	RTC and CMOS I/O voltage supply	Vmax=1.89V Vmin=1.71V Vnom=1.8V $I_{VIO/RTC}$=15uA@ Hibernate mode	Power supply for RTC and CMOS I/O. In the full on mode, make sure both VIO/RTC and VCC simultaneously power on. In the hibernate mode, make sure VIO/RTC powers on to keep the data lossless.
General purpose input/output					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
RESET	23	I	External reset input, active low	VILmin=-0.4V VILmax=0.45V VIHmin=0.7* VIO/RTC VIHmax=3.6V	The system reset is provided by the RTC monitor circuit and it is active low and must have an external pull up resistor to keep the signal stable when it works. If unused, leave this pin unconnected.
EINT0	5	I	External interrupt input pin, which is only a level triggered interrupt.	VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	If unused, pull this pin down to ground directly. It is not supported by SIRF at present.

ON_OFF	4	I	Power control pin	VILmin=-0.4V VILmax=0.45V VIHmin=0.7* VIO/RTC VIHmax=3.6V	A pulse generated on the ON_OFF pin which lasts for at least 1ms and consists of a rising edge and low level, can switch operating mode between hibernate and full-on.
1PPS	3	O	One pulse per second	VOLmin=-0.3V VOLmax=0.4V VOHmin=0.75*VCC	1PPS output provides a pulse signal for time purpose. If unused, leave this pin unconnected.
Serial Interface					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
DR_I2CDIO	21	I/O	Dead Reckoning I2C data (SDA)	VOLmax=0.4V VOHmin=0.75*VCC VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	If unused, leave this pin unconnected.
DR_I2C_CLK	22	O	Dead Reckoning I2C clock(SCL)	VOLmax=0.4V VOHmin=0.75*VCC	If unused, leave this pin unconnected.
CFG0/ SCK	17	I	Function overlay: ● SPI_CLK slave SPI clock input (SCK) ● Configure Pin 0	VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	When serial port is configured as UART, pull up to VCC via a 10k resistor.
CFG1/ SCS	18	I	Function overlay: ● SPI_CS_N slave SPI chip select (SCS) active low ● Configure Pin 1	VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	When serial port is configured as I2C, pull down to GND via a 10k resistor.

RXD/ MOSI/ SDA	20	I/ O	Function overlay: ● SSPI_DI slave SPI data input (MOSI) ● UART_RX UART data receive (RXD) ● I2C_DIO I2C data (SDA)	VOLmax=0.4V VOHmin=0.75*VCC VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	
TXD/ MISO/ SCL	19	I/ O	Function overlay: ● SSPI_DO slave SPI data output (MISO) ● UART_TX UART data transmit (TXD) ● I2C_CLK I2C clock (SCL)	VOLmax=0.4V VOHmin=0.75*VCC VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	
Others					
PIN NAME	**PIN NO.**	**I/ O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
GND	6,7,9, 10,11 ,12, 13,14 ,15, 24		Ground		
Reserved	8,16				Reserved

3.3 Operating Modes

The table below briefly summarizes the various operating modes in the following chapters.

Table 6: Overview of operating modes

Mode	Function
Acquisition mode	The module starts to search satellites and determine visible satellites，coarse carrier frequency and code phase of satellite signals. When the acquisition is completed, it switches to tracking mode automatically.
Tracking mode	The module refines acquisition's message, as well as keeping tracking and demodulating the navigation data from the specific satellites.
Hibernate mode	The module can be switched to hibernate mode by applying a pulse which consists of a rising edge and high level that persists for at least 1ms on the ON_OFF pin.

3.4 Power Management

There are two power supply pins in L50, VCC and VIO/RTC.

3.4.1 VCC Power

VCC pin supplies power for GPS BB domain and GPS RF domain. The power supply VCC's current varies according to the processor load and satellite acquisition. Typical VCC max current is 100 mA. So it is important that the power is clean and stable. Generally, ensure that the VCC supply ripple voltage meet the requirement: 54 mV(RMS) max @ f = 0~3MHz and 15 mV(RMS) max @ f > 3 MHz.

Table 7: Pin definition of the VCC pin

Name	Pin	Function
VCC	2	power supply for GPS BB and RF part

3.4.2 VIO/RTC Power

The VIO/RTC pin supplies power for all RTC domain and CMOS I/O domain, so VIO/RTC should be powered all the time when the module is running. It ranges from 1.71V to 1.89V. In order to achieve a better Time To First Fix (TTFF) after VCC power down, VIO/RTC should be valid all the time. It can supply power for SRAM memory which contains all the necessary GPS information for quick start-up and a small amount of user configuration variables.

Table 8: Pin definition of the VIO/RTC pin

Name	Pin	Function
VIO/RTC	1	Power for RTC and CMOS /IO

3.4.3 Energy Saving Mode

3.4.3.1 ATP Mode

Adaptive trickle power (ATP): In this mode, L50 cycles three modes internally to optimize power consumption. These three modes consist of full on mode, CPU only mode and standby mode. The full on mode lasts about 200~900ms to require new ephemeris to get a valid position, and the other two modes are partially power off or completely power off to decrease power consumption. The timing sequence is shown in following figure. This mode is configurable with SiRF binary protocol message ID151. The following diagram is a default configuration and it is tested in the strong signal environment. When the signal becomes weak, it will not comply with the following rule. The weaker the signal is, the longer time the module lasts in full on mode. In the extreme condition, when there is no signal input, the mode cycles only two modes, which are full on and standby mode.

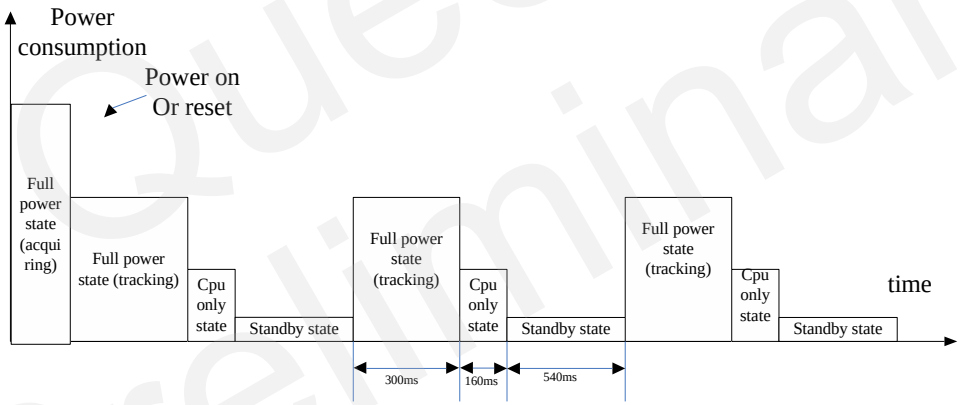


Figure 2: ATP timing sequence

3.4.3.2 PTF Mode

Push to fix (PTF): In this mode, L50 is configured to be waked up periodically, typically every 1800 sec (configurable range 10~7200 sec) for updating position and collecting new ephemeris data from valid satellites. For the rest of the time, the module stays in Hibernate mode. A position request acts as a wakeup of the module, which is then able to supply a position within the hot-start time specification.This mode is configurable with SiRF binary protocol message ID167 and the following figure is the default configuration. Additionally, when the signal becomes weak, pushing to fix function is not valid.

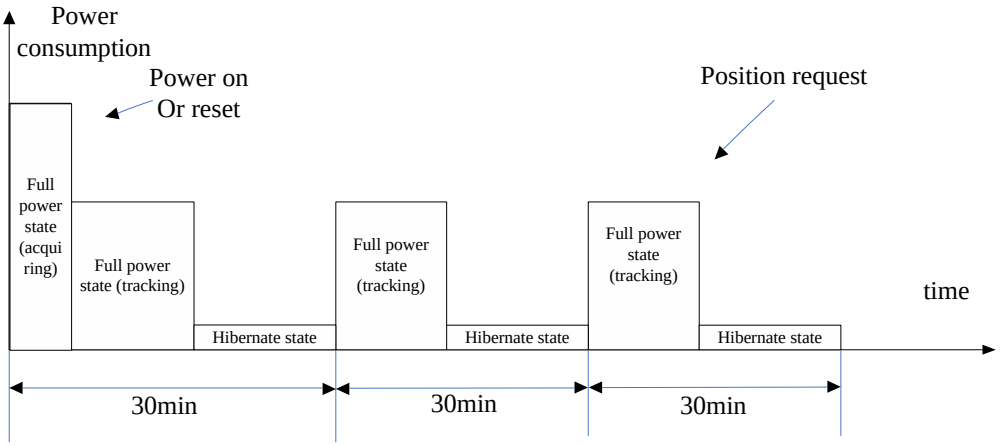


Figure 3: PTF timing sequence

3.4.3.3 Hibernate Mode

Hibernate mode means low power consumption in this mode. Some power domains are powered off such as ARM, DSP and RF part, but the RTC domain includes all non-volatile logic, and the RAM, and GPS BB logic I/O are still active. The module is woken up from Hibernate mode on the next ON_OFF (at rising edge) using all internal aided information like GPS time, Ephemeris, Last Position and so on, to carry out a fast TTFF in either Cold or Warm start mode.

3.5 Power Supply

3.5.1 Power Reference Design

The following diagram is one solution of power supply for L50 module. Customers can follow this reference design to get a short TTFF in either warm start or cold start. One concern of this design is that the battery will take the place of VCC_3.3 to supply power for RTC and CMOS I/O of the module when VCC_3.3 is absent. Furthermore, VCC_3.3 will charge the battery when it is active.

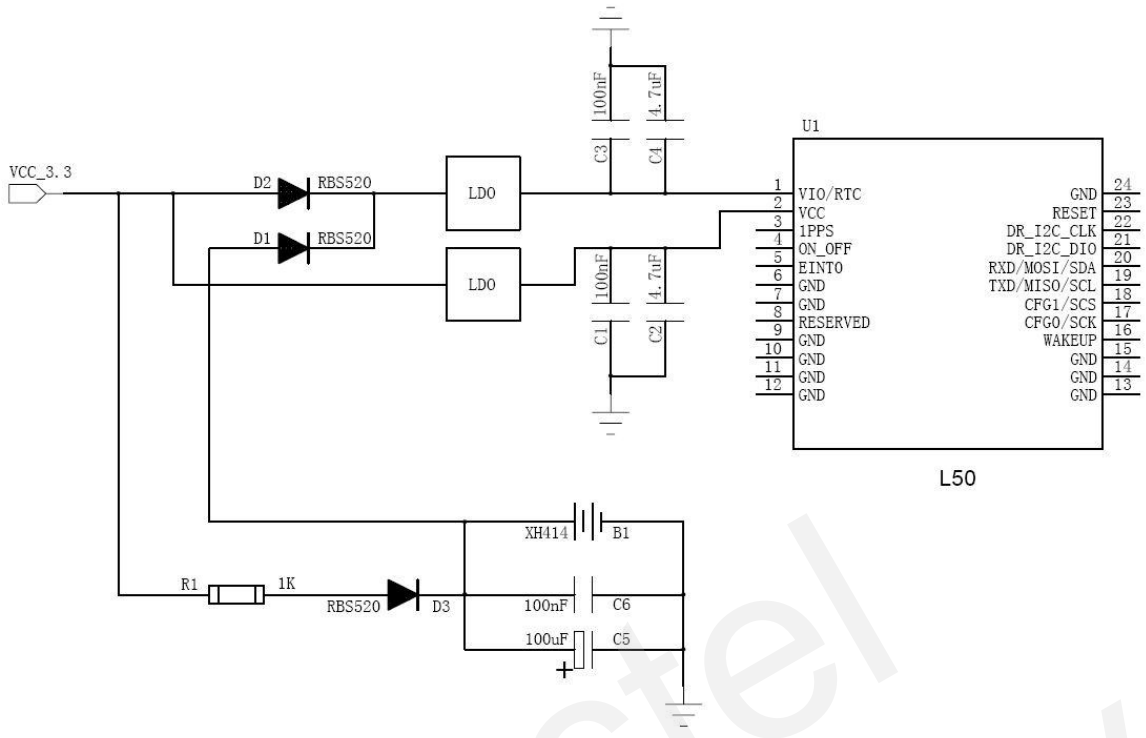


Figure 4: Power design reference for L50 module

3.5.2 Battery

In this part, the charging circuit of battery is introduced and XH414 is chosen as an example, the following circuit is the reference design.

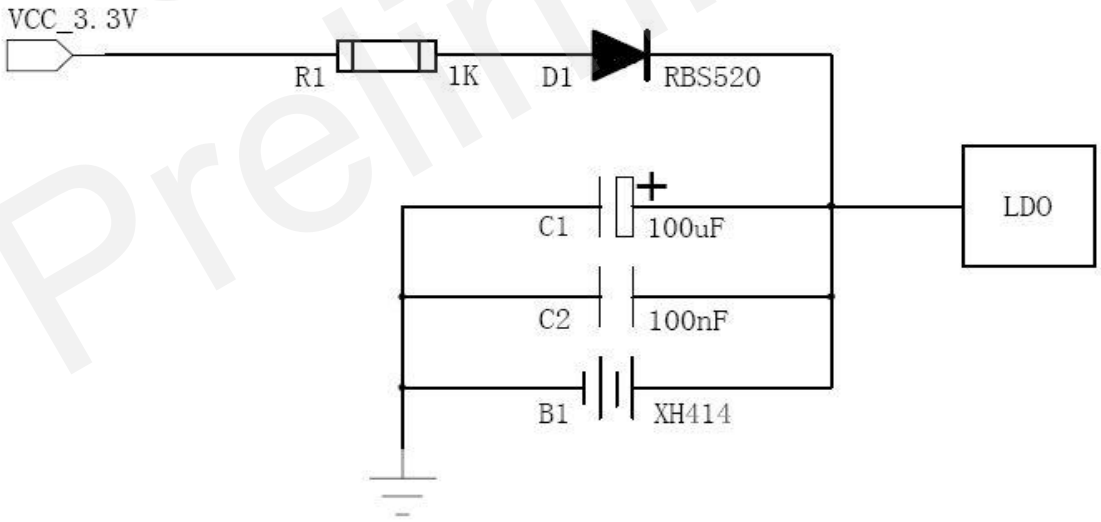


Figure 5: Reference charging circuit for chargeable battery

Coin-type Rechargeable Capacitor such as XH414H-IV01E from Seiko can be used and Schottky diode such as RB520S30T1G from ON Semiconductor is recommended for its low voltage drop. The charging and discharging characteristic of XH414 is shown in the following figure.

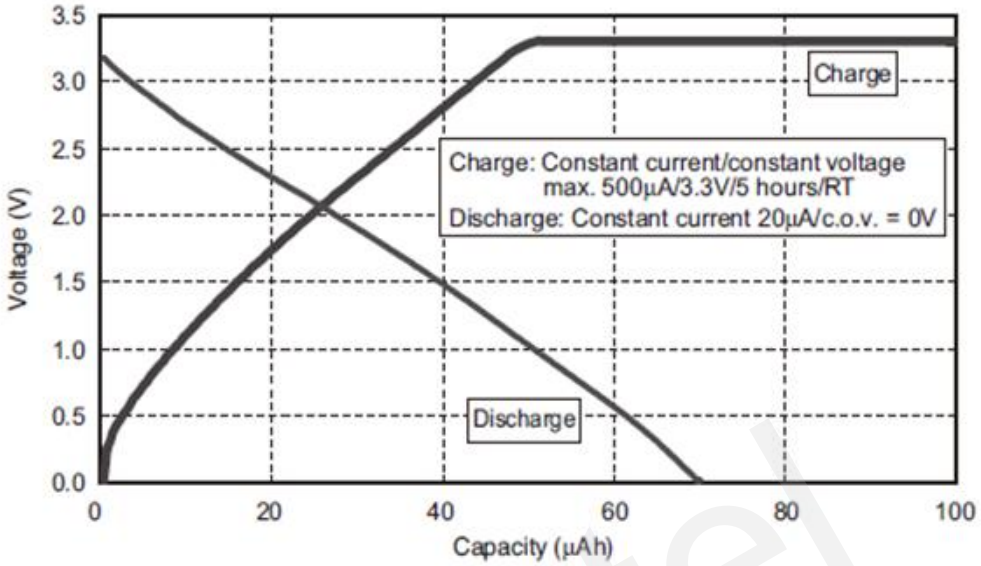


Figure 6: Seiko XH414 charging and discharging characteristics

3.6 Timing Sequence

The ON_OFF pin is used to switch the module between full-on mode and hibernate mode.

L50 integrates power on reset circuit internally and external RESET signal which belongs to VIO/RTC domain. When VCC and VIO/RTC are supplied simultaneously, the internal power on reset circuit executes. Normally, external control of RESET is not necessary. When power supply VCC is removed abruptly, an external RESET is suggested. Additionally, make sure the external RESET pin is pulled up to VCC via a 10K resistor.

The following diagram is the reference timing sequence. Firstly, VCC and VIO/RTC power on ,then a pulse of wakeup will be generated , after that when ON/OFF is toggled ,the module will go into the full on mode and the WAKEUP will turn to high level. Next toggling of the ON/OFF will make the module return to the hibernate mode. The state conversion is shown in the following figure.

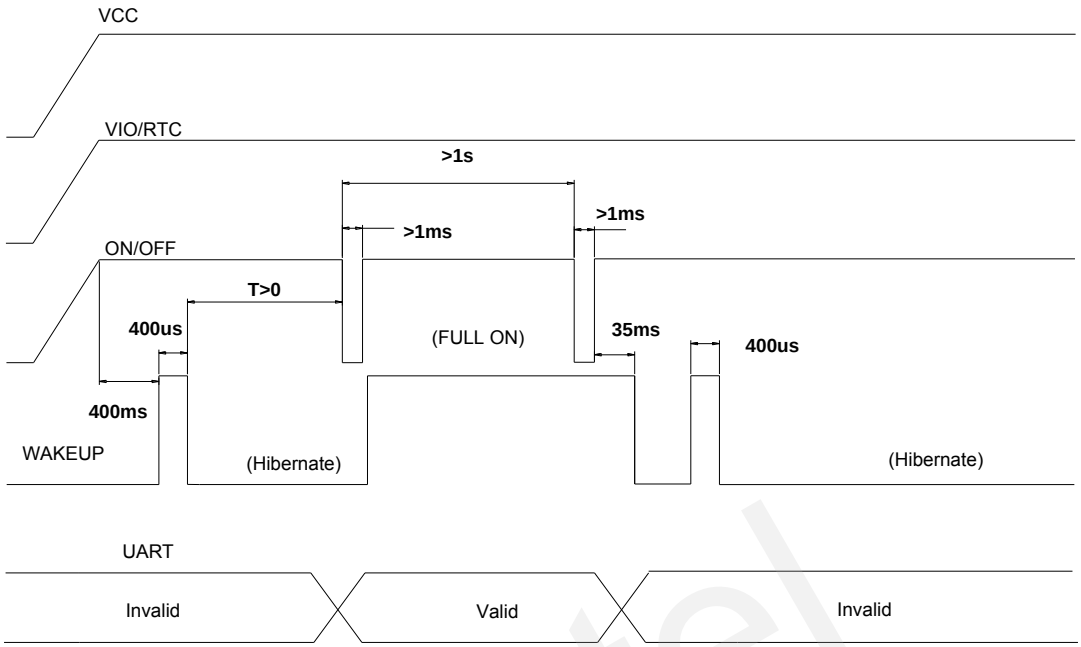


Figure 7: Turn on timing sequence of module

NOTE:

If the "ON_OFF" pin is controlled by host controller, a 1KΩ resistor should be inserted between the GPIO of the controller and "ON_OFF" pin.

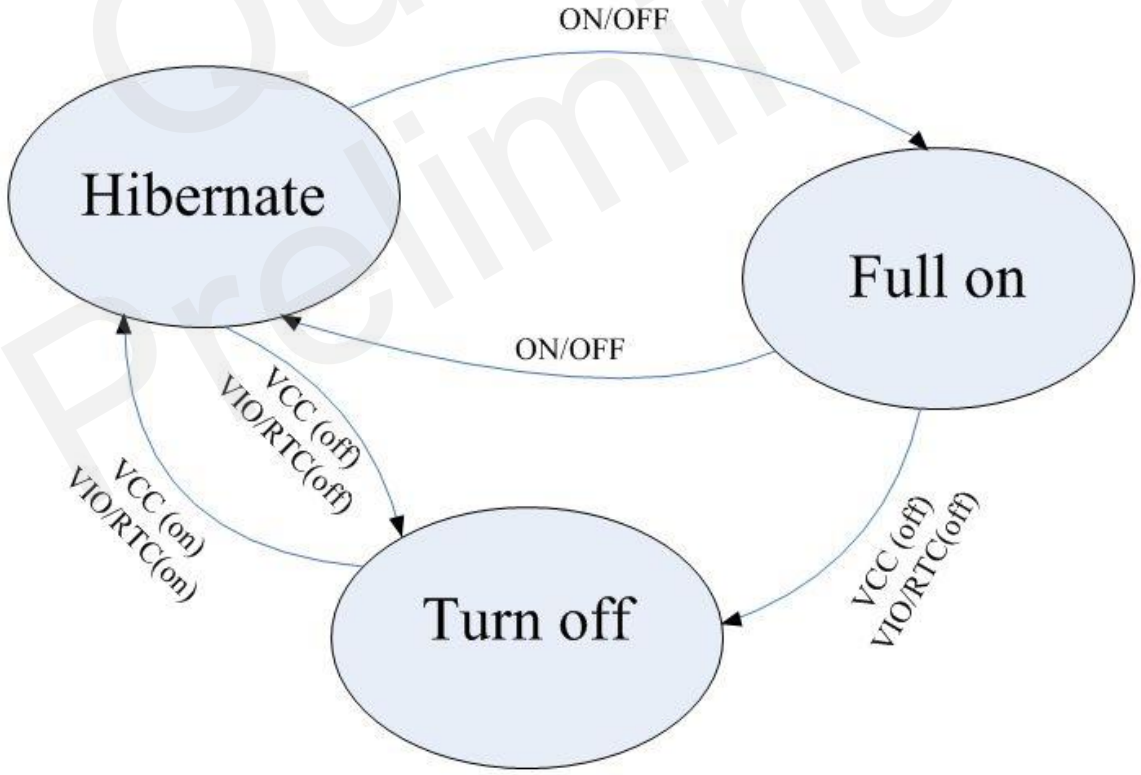


Figure 8: State conversion of module

3.7 Communication Interface

Communication interface which includes UART interface/ I2C interface/ SPI interface is used to output NMEA messages or to communicate with the customer's device via the OSP protocol. All these interfaces are multiplexed on a share set of pins. The interface selection is not intended to be changed dynamically but only at boot time.

Table 9: Multiplexed function pins for communication interface

Pin name	Pin NO.	Communicate interface	
		UART	I2C
CFG0/SCK	17	Pull up	Open
CFG1/SCS	18	Open	Pull down
RXD/MOSI/SDA	20	Data receive	I2C data (SDA)
TXD/MISO/SCL	19	Data transmit	I2C clock (SCL)

3.7.1 UART Interface

L50 offers multiplexed pins which can be configured as one UART interface and CFG0/SCK should be pulled up to VCC via a 10K resistor. The module is designed as a DCE (Data Communication Equipment). Serial port TXD/MISO/SCL is connected to UART RX of customer's device, while serial port RXD/MOSI/SDA is connected to UART TX of customer's device. It supports data baud rate from 4800bps to 115200bps, meanwhile customers can change the baud rate by SIRF binary protocol message ID 134.

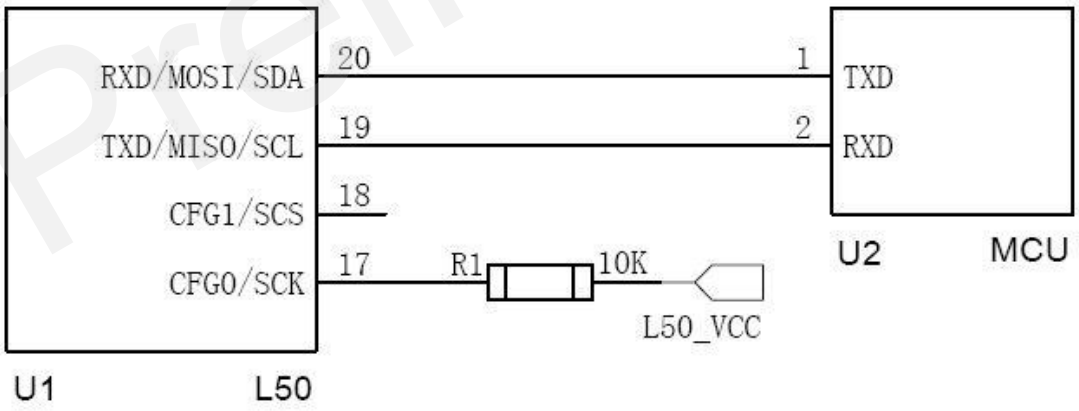


Figure 9: UART design reference for L50 module

This UART interface has the following features:

- The UART interface can be used to output NMEA and input & output OSP messages.
  The default output NMEA types are **RMC, GGA, GSA, and GSV (after successful positioning).**
- The UART interface supports the following data rates:
  4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200.
  The default setting is 4800bps, 8 bits, no parity bit, 1 stop bit, no hardware flow control.
- The output is CMOS 1.8V compatible and the input is 3.6V tolerant.

Note: It is strongly recommended that the UART interface is used to output NMEA message to serial port of host processor.

The UART interface does not support the RS-232 level. It supports only the TTL/CMOS level. If the module UART interface is connected to the UART interface of a computer, it is necessary to insert a level shift circuit between the module and the computer. Please refer to the following figure.

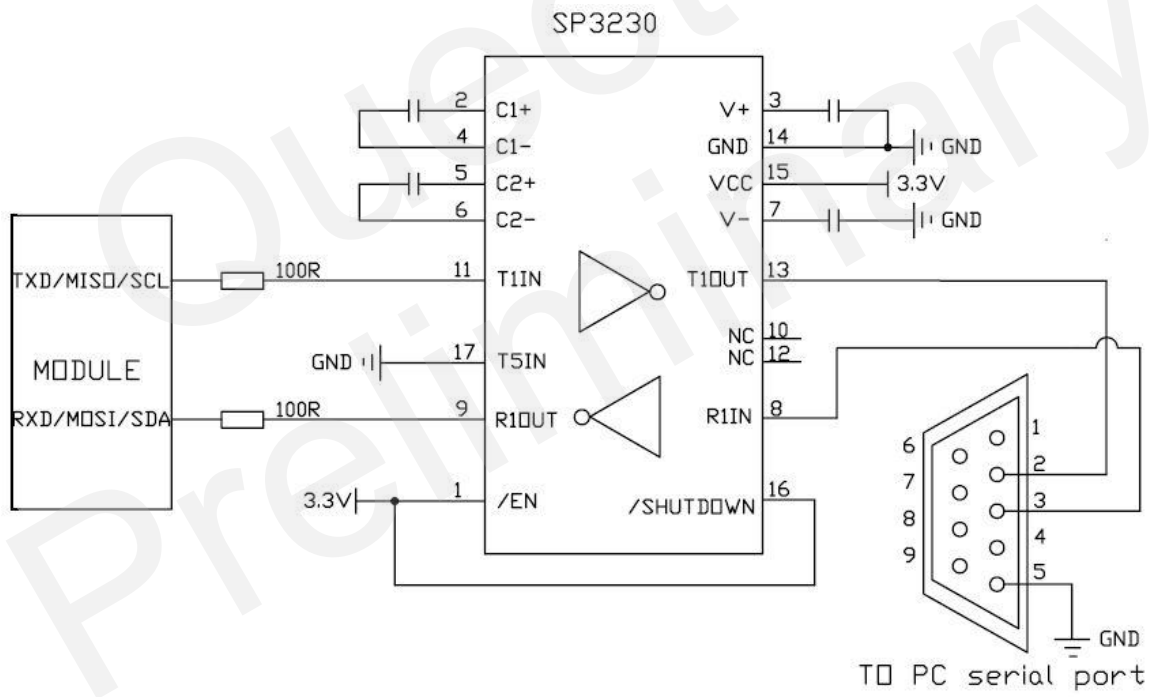


Figure 10: RS-232 level shift circuit

3.7.2 I2C Interface

L50 provides multiplex function via TXD/MISO/SCL, RXD/MOSI/SDA and CFG1/SCS to construct I2C interface. Communication interface is configured as I2C by pulling CFG1/SCS down via the resistor R1. The default mode is master mode. It is important that the customer must pull up these two pins via 2K resistor for the OC/OD interface. Otherwise, there is no signal output. The reference design is described in Figure 12.

This I2C interface has the following features:

- Operate up to 400kbps.
- Support Multi-master I2C mode by default.
- The default I2C master address: 0x60.
- The default I2C slave address: 0x62.

The following figure is the I2C timing sequence.

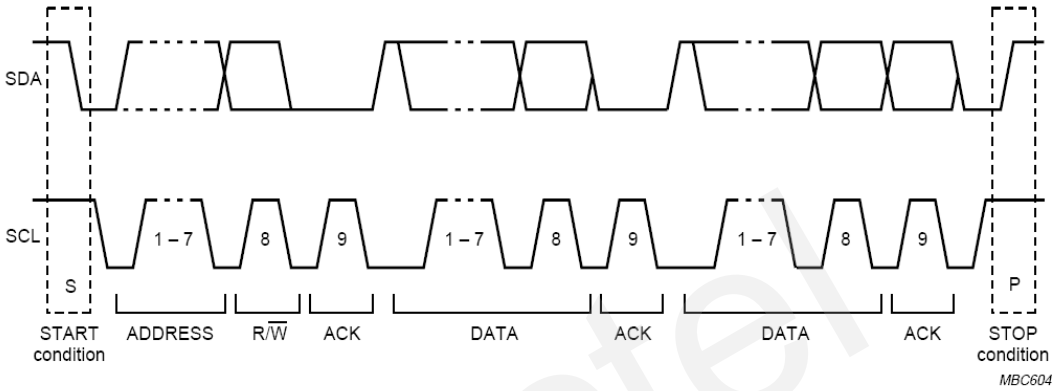


Figure 11: I2C timing sequence

The following circuit is an example of connection.

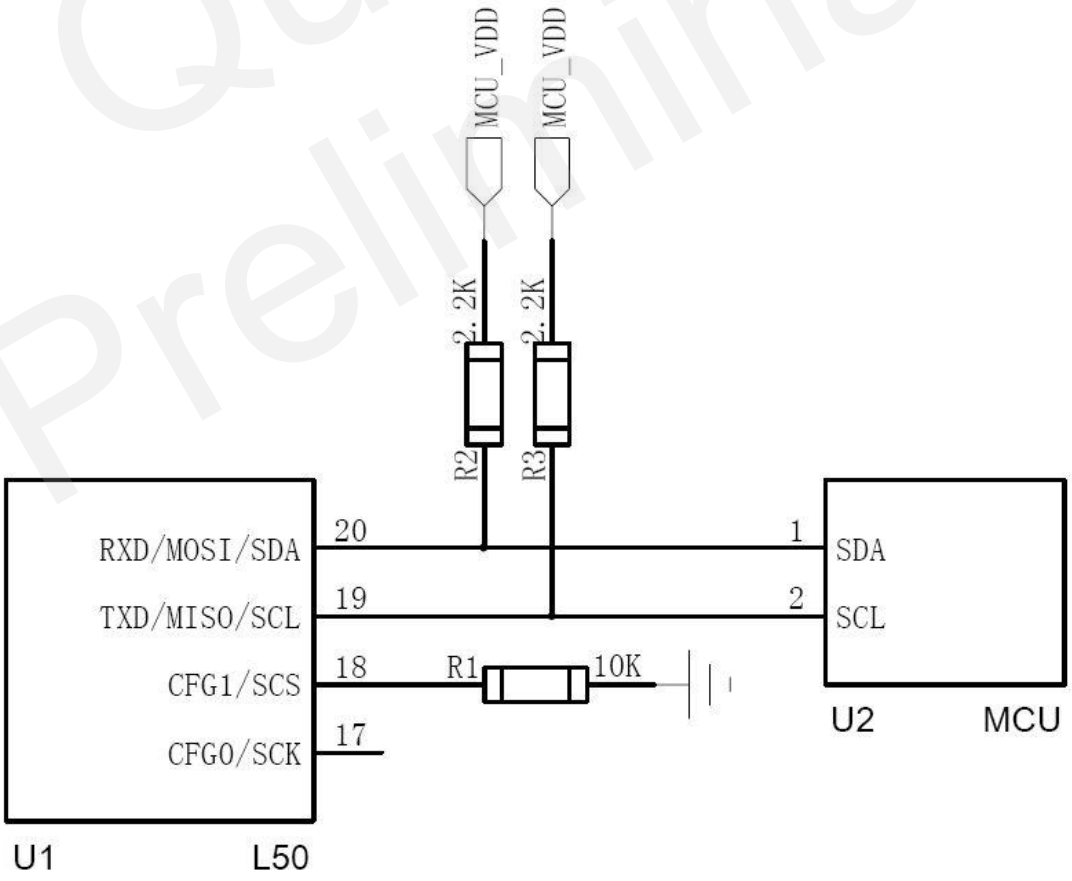


Figure 12: I2C design reference for L50 module

3.7.3 SPI Interface

The Serial Peripheral Interface (SPI) provides access to a flexible, full-duplex synchronous serial bus. However, L50 doesn't support SPI at present.

3.8 Assisted GPS

By supplying aided information like ephemeris, almanac, rough last position, time and satellite status, A-GPS can help improve TTFF and the acquisition sensitivity of the GPS receiver.

L50 supports one kind of A-GPS called Client Generated Extended Ephemeris (CGEE) which ensures fast TTFF out to 3 days .The CGEE data is generated internally from satellite ephemeris as a background task, and then L50 collects ephemeris from as many satellites as possible before entering Hibernate mode.

The CGEE functionality requires that VIO/RTC power supply is kept active all the time and an external 1Mbit EEPROM connected to DR_I2C bus for CGEE data storage. The recommended EEPROMs are in the following table and they are verified.

Table 10: Recommended EEPROMs

Manufacturer	Part Number
ST	M24M01
Seiko Instruments Inc.	S-24CM01C
Atmel	AT24C1024B

Note: The part number which we recommend is a series part number, please get more details from the datasheet such as operation voltage and package.

Table 11: Pin definition of the DR_I2C interfaces

Interface	Name	Pin	Function
Dead Reckoning I2C Interface	DR_I2C_DIO	21	I2C data (SDA)
	DR_I2C_CLK	22	I2C clock (SCL)

The DR_I2C_DIO and DR_I2C_CLK pins are open-drain output and should be pulled up to VDD which depends on the EEPROM's operation voltage externally by 2K resistors to meet requirement of maximum data rate up to 400Kbs. The following circuit is the reference design for L50 and EEPROM.

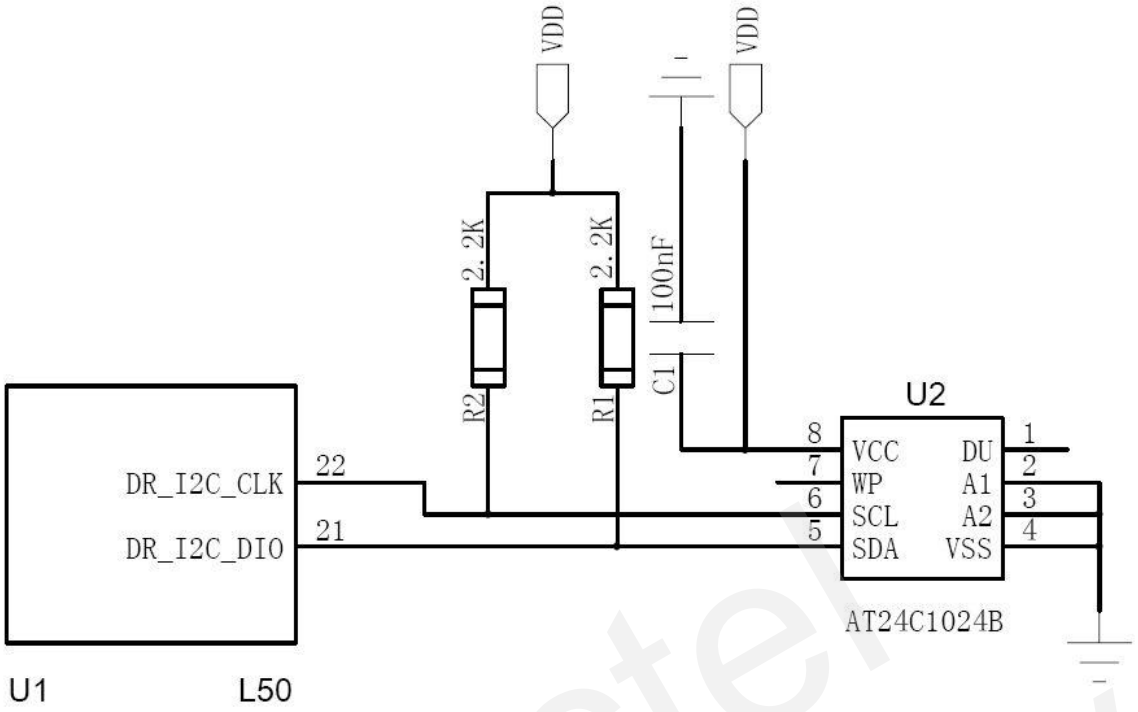


Figure 13: Reference design for CGEE function

4. Radio Frequency

L50 receives L1 band signal from GPS satellites at a nominal frequency of 1575.42MHz. It is an ultra slim module with embedded 15 × 15 × 2.0mm patch antenna. Alongside highest reliability and quality of patch antenna, L50 also offers 48 PRN channels, which allows the module to acquire and track satellites in the shortest time, even at a very low signal level.

4.1 Antenna

The quality of the GPS antenna chosen is crucial to the overall sensitivity of the GPS system. L50 offers an on-module patch antenna, which help customers reduce the period of new product development greatly. A 15 × 15 × 2.0mm patch antenna is chosen for reducing product size. This antenna is specially designed for satellite reception applications. And this patch antenna has excellent stability and sensitivity to consistently provide high signal reception efficiency. The specification of the antenna used by L50 is described in the table below.

Table 12: Antenna specification for L50 module

Antenna type	Parameter	Specification	Notes
Patch antenna	Size	15×15×2.0mm	
	Center Frequency	1577MHz±3MHZ	
	Impendence	50 Ohm	
	Band Width	>9 MHz	Return Loss ≦-10dB
	Frequency Temperature Coefficient (TF)	0±20ppm/℃	-40℃-150℃
	Polarization	RHCP	Right Hand Circular Polarization
	Gain at Zenith	-2.0dBic typ.	Center frequency
	VSWR	1.5 max	
	Axial ratio	3 dB max	

Notes: L50 can also support a 18×18×2.0mm patch antenna.

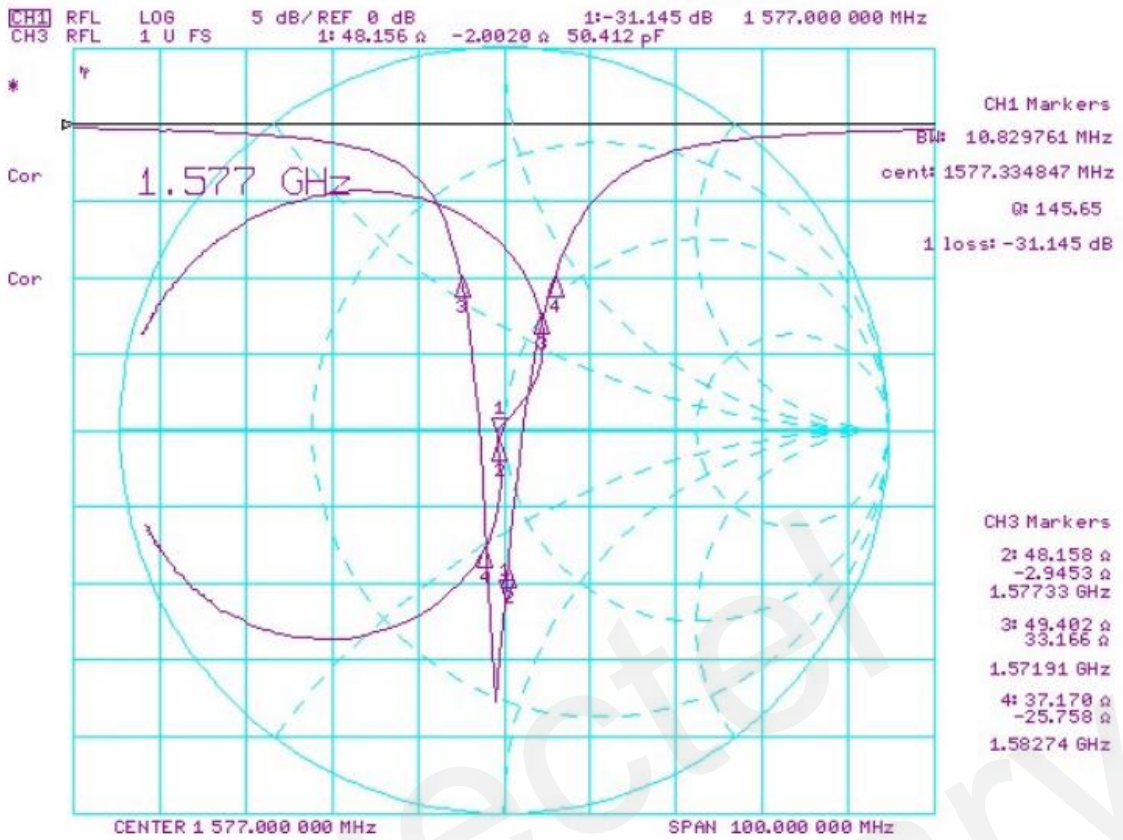


Figure 14: Patch antenna test result

4.2 Design notice

Theoretically the best position for L50 module is not only in the center of PCB not also is on the top of the PCB, so the radiation plots won't be skewed due to the effects of placing it close to the edge of the PCB. The larger the ground-plane is, the higher the gain is in general. And the center frequency of the antenna will been changed based on the size of the ground-plane. It strongly recommended that the host PCB is bigger than 80×40mm.

Keep the antenna upside for better performance and remove obstacle between antenna and GPS satellites. For example, a metal cover should not be used over the antenna.
The evaluation board is as follows.

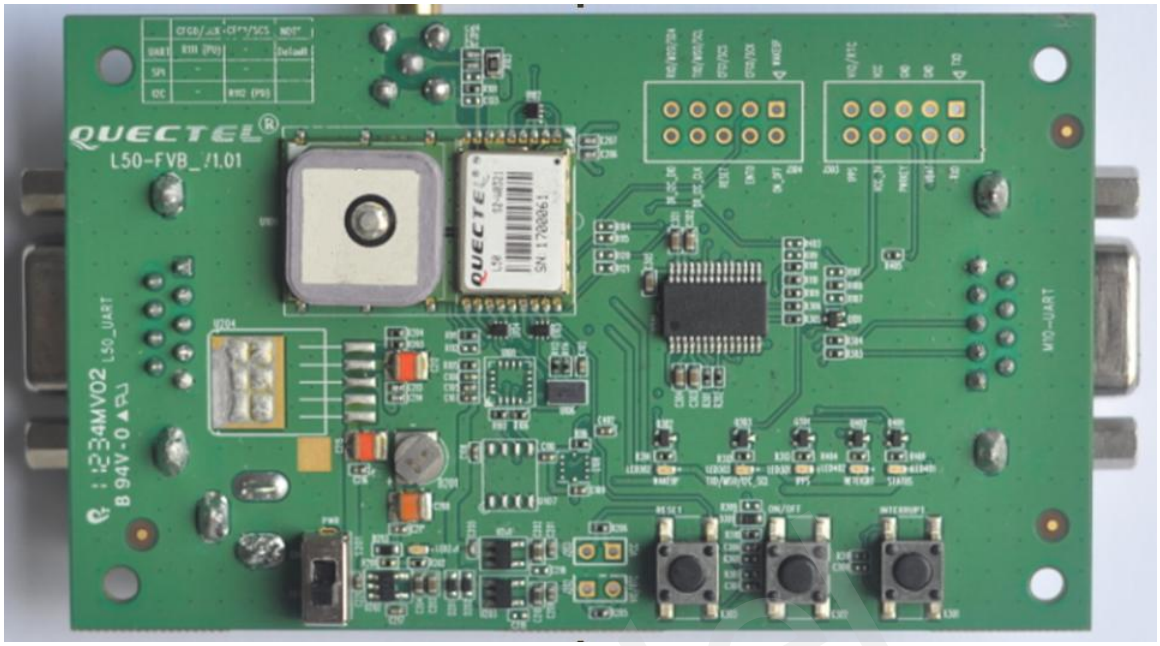


Figure 15: EVB of L50

5. Electrical, Reliability and Radio Characteristics

5.1 Absolute Maximum Ratings

Absolute maximum rating for power supply and voltage on digital pins of the module are listed in the following table.

Table 13: Absolute maximum ratings

Parameter	Min	Max	Unit
Power supply voltage （VCC）	-0.3	2	V
Backup battery voltage (VIO/RTC)	-0.3	2	V
Input voltage at digital pins	-0.5	3.6	V
Storage temperature range	-45	125	℃

Note: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. The product is not protected against over voltage or reversed voltage. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

5.2 Operating Conditions

Table 14: Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
VCC	Supply voltage	Voltage must stay within the min/max values, including voltage drop, ripple, and spikes.	1.71	1.8	1.89	V
I_{VCC}	Peak supply current	VCC=1.8V@-140dBm	—	—	54	mA
VIO/RTC	Backup voltage supply		1.71	1.8	1.89	V
$I_{VIO/RTC}$	Backup battery current	VIO/RTC=1.8V In hibernate mode	—	20	—	uA
T_{OPR}	Normal Operating temperature		-40	25	85	℃

Note: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

5.3 Current Consumption

Table 15: The module current consumption

Parameter	Condition	Min	Typ	Max	Unit
Itotal Acquisition	Open sky @-130dBm	-	45	-	mA
Itotal Tracking	Open sky@-130dBm	-	35	-	mA
Hibernate		-	20	-	uA

Note: Itotal=Ivcc+Ivio/rtc

5.4 Electro-Static Discharge

L50 module has better ESD performance, because every pin is protected by a transient voltage suppressor (TVS). However, ESD protection precautions should still be emphasized. Proper ESD handing and packaging procedures must be applied throughout the processing, handing and operation of any application.

The ESD bearing capability of the module is listed in the following table. Note that the customer should add ESD components to module pins in practical application except VCC and GND pins.

Table 16: The ESD endurance table (Temperature: 25℃, Humidity: 45 %)

Pin	Contact discharge	Air discharge
VCC, GND，Patch antenna	±5KV	±10K
Others	±4KV	±8K

5.5 Reliability Test

Table 17: Reliability test

Test term	Condition	Standard
Thermal shock	-30℃...+80℃, 144 cycles	GB/T 2423.22-2002 Test Na IEC 68-2-14 Na
Damp heat, cyclic	+55℃; >90% Rh 6 cycles for 144 hours	IEC 68-2-30 Db Test
Vibration shock	5~20Hz,0.96m^2/s^3;20~500Hz,0.96m^2/s^3-3dB/ oct, 1hour/axis; no function	2423.13-1997 Test Fdb IEC 68-2-36 Fdb Test
Heat test	85℃, 2 hours, Operational	GB/T 2423.1-2001 Ab IEC 68-2-1 Test
Cold test	-40℃, 2 hours, Operational	GB/T 2423.1-2001 Ab IEC 68-2-1 Test
Heat soak	90℃, 72 hours, Non-Operational	GB/T 2423.2-2001 Bb IEC 68-2-2 Test B
Cold soak	-45℃, 72 hours, Non-Operational	GB/T 2423.1-2001 A IEC 68-2-1 Test

6. Mechanical Dimensions

This chapter describes the mechanical dimensions of the module.

6.1 Mechanical Dimensions of the Module

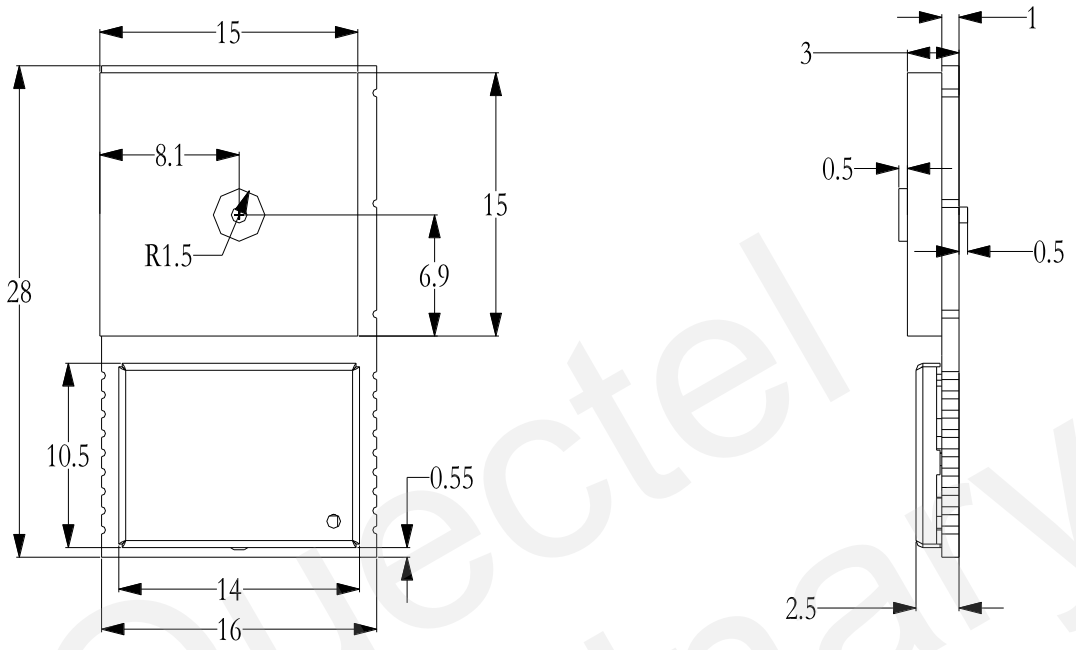


Figure 16: L50 Top view and Side view（Unit:mm）

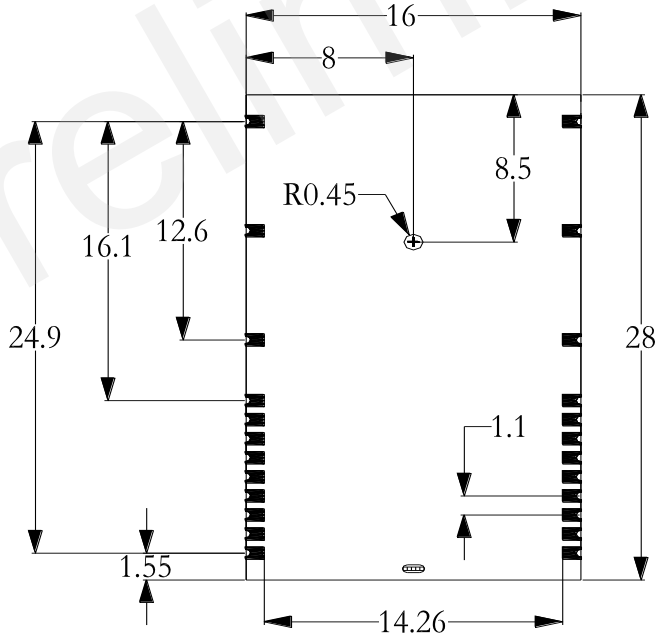


Figure 17: L50 Bottom view（Unit:mm）

6.2 Recommended Footprint

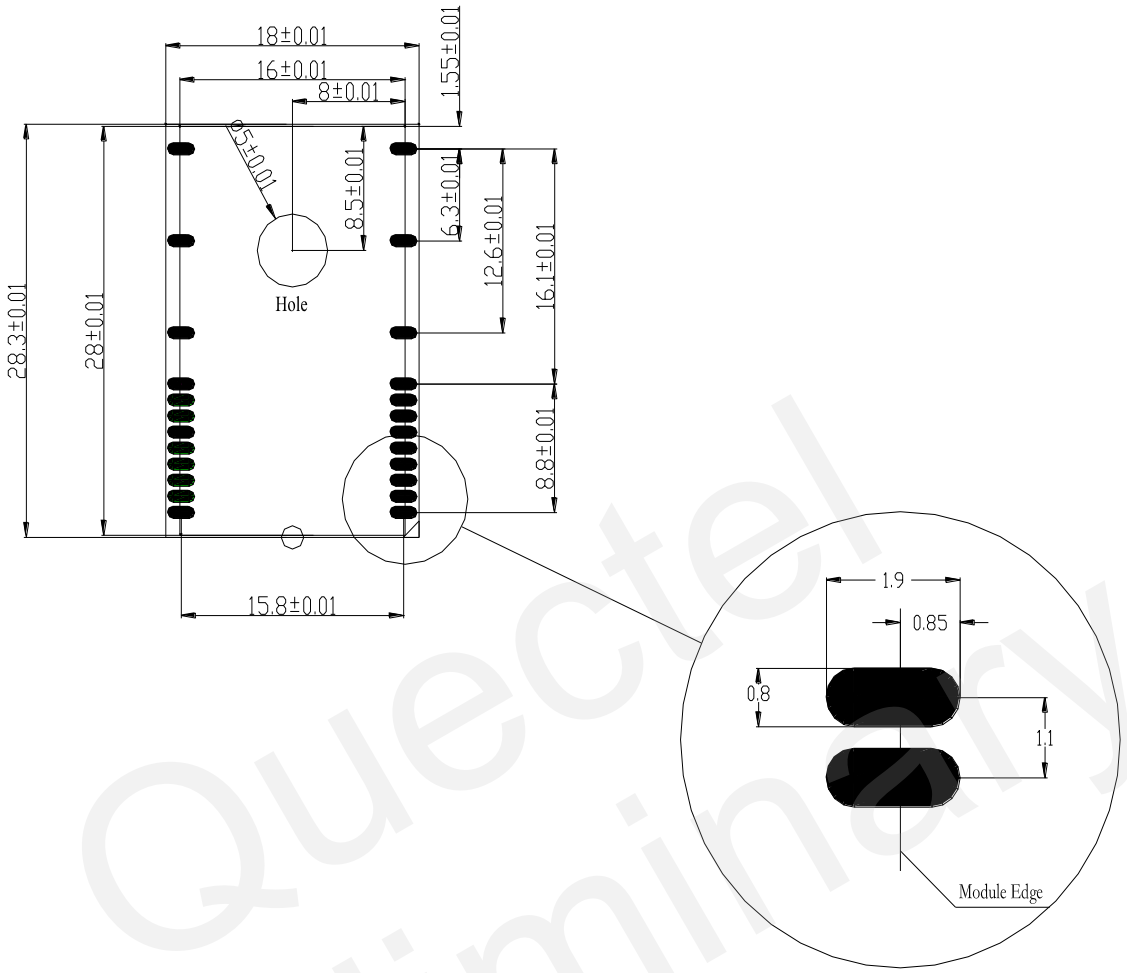


Figure 18: Recommended Footprint （Unit:mm）

6.3 Top View of the Module

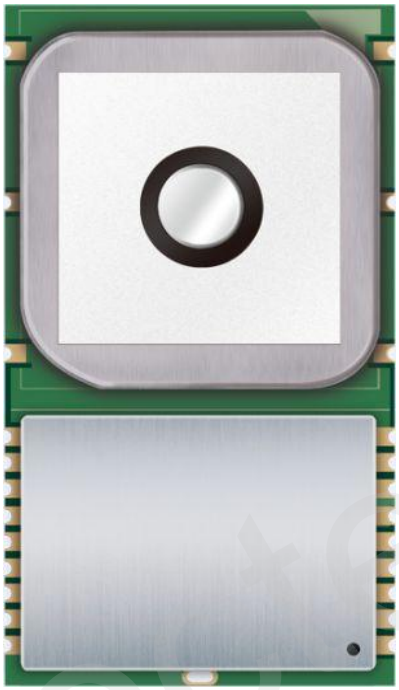


Figure 19: Top view of module

6.4 Bottom View of the Module

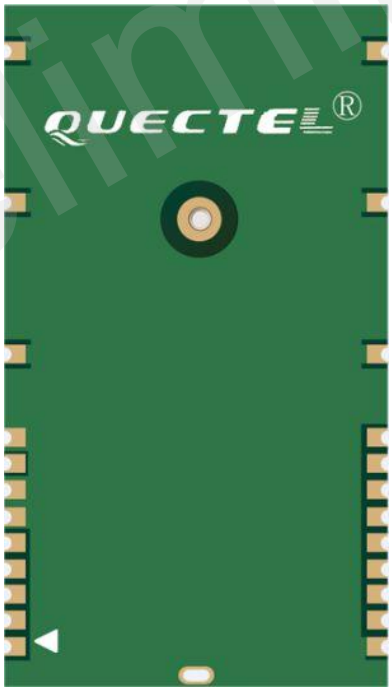


Figure 20: Bottom view of module

7. Manufacturing

7.1 Assembly and Soldering

L50 is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. It is suggested that the minimum height of solder paste stencil is 130um to ensure sufficient solder volume. Pad openings of paste mask can be increased to ensure proper soldering and solder wetting over pads. It is suggested that peak reflow temperature is 235~245℃ (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260℃. To avoid damage to the module when it is repeatedly heated, it is suggested that the module should be mounted after the first panel has been reflowed. The following picture is the actual diagram which we have operated.

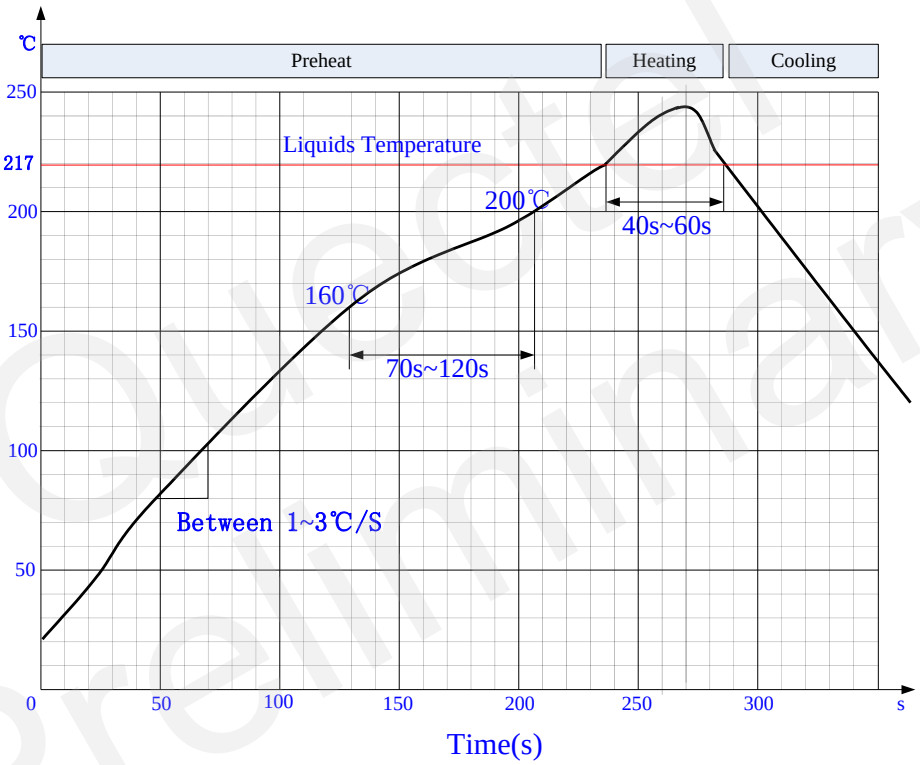


Figure 21: Ramp-soak-spike-reflow of furnace temperature

7.2 Moisture Sensitivity

L50 is sensitive to moisture absorption. To prevent L50 from permanent damage during reflow soldering, baking before reflow is required in following cases:

- Humidity indicator card: At least one circular indicator is no longer blue.
- The seal is opened and the module is exposed to excessive humidity.

L50 should be baked for 192 hours at temperature 40℃+5℃/-0℃ and <5% RH in low-temperature containers, or 24 hours at temperature 125℃±5℃ in high-temperature containers. Care should be

taken that plastic tray is not heat resistant. L50 should be taken out before preheating, otherwise, the tray may be damaged by high-temperature heating.

7.3 ESD Safe

L50 module is an ESD sensitive device and should be handled carefully.

7.4 Tape and Reel

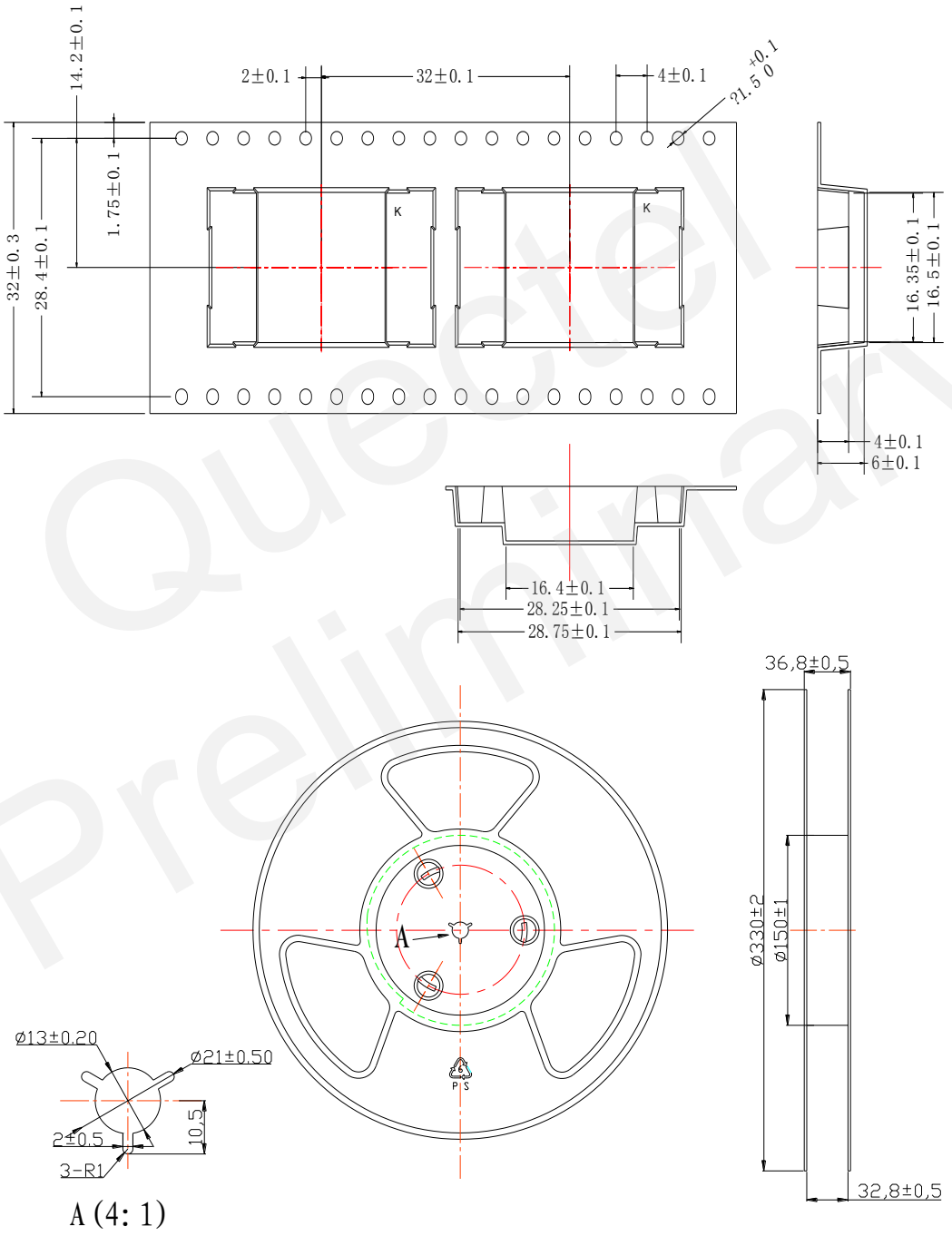


Figure 22: Tape and reel specification

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