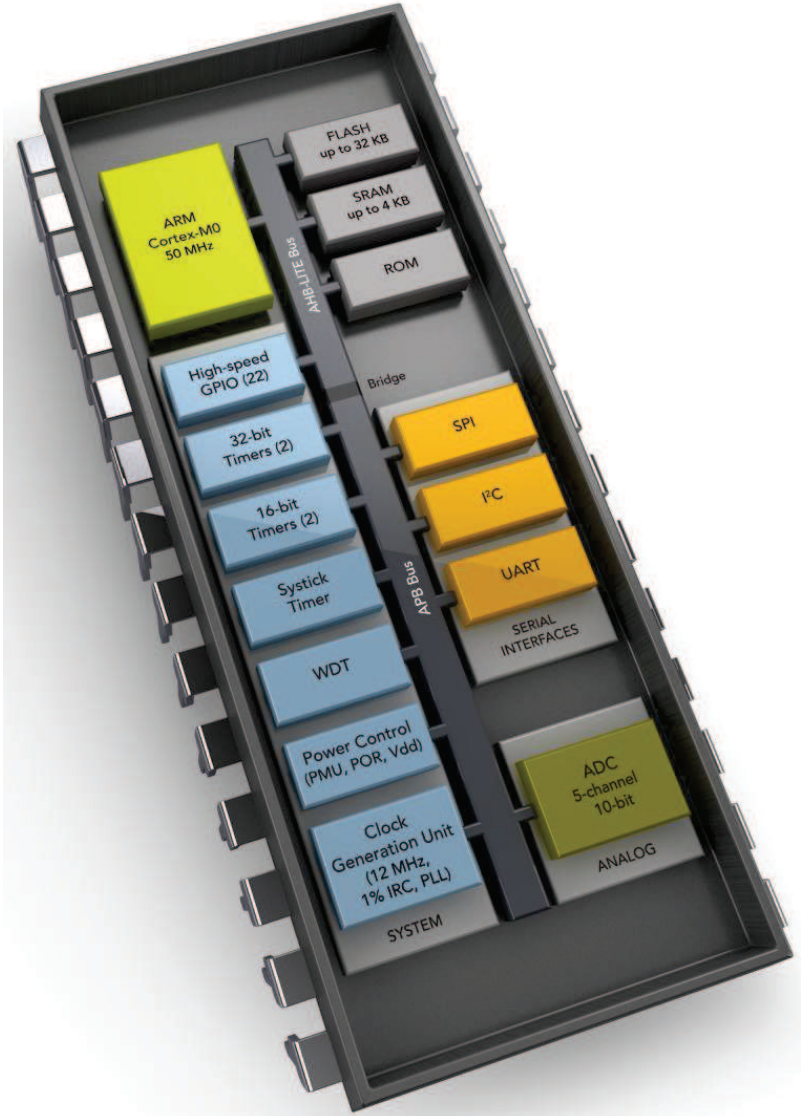
LPC1100L in Low-Pin-Count Packages



- Cortex-M0 Core up to 50MHz
- **Lowest** Active Current 130uA/MHz
- Memory:
  - Up to 32 KB on-chip Flash
  - Up to 4 KB SRAM
- Peripherals:
  - U(S)ART, SPI/SSP, I2C
  - 4x general purpose Timers with PWM
  - 10-bit 5-channel ADC
  - Programmable WDT and oscillator
  - 1% accuracy, 12 MHz IRC oscillator
- Single 3.3 V power supply (1.8 V to 3.6 V)
- SO, TSSOP, DIP package options

Important Features for 8/16-bit MCU Customers

- **Timers with PWM Generation** – For each timer, up to four match registers can be configured as PWM, each timer supports up to three match outputs as single edge controlled PWM outputs;
- **Dynamic System Clock Switching** – Change frequency on the fly depending on processing demand. The LPC1100 current consumption at 50 MHz is specified at 7mA. This can be reduced to a little over 130uA when running at 1 MHz on the low-power internal oscillator;
- **Clock Output** – Clock output with divider can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock. Output can source downstream devices such as other microcontrollers, CPLD or FPGA;
- **Interrupt via Any GPIO** – Any GPIO pins can be used as Edge and Level Sensitive interrupt sources;
- **Programmable Pull Up/Down/Open Drain** – Internal pull-up/pull-down resistor, pseudo open drain or bus keeper function;
- **Enhanced GPIO Pin Manipulation** – Capable of simultaneously reading Bit/Byte/Word or toggling up to 22 I/Os per instruction

Low-Pin-Count Package Options

SO20

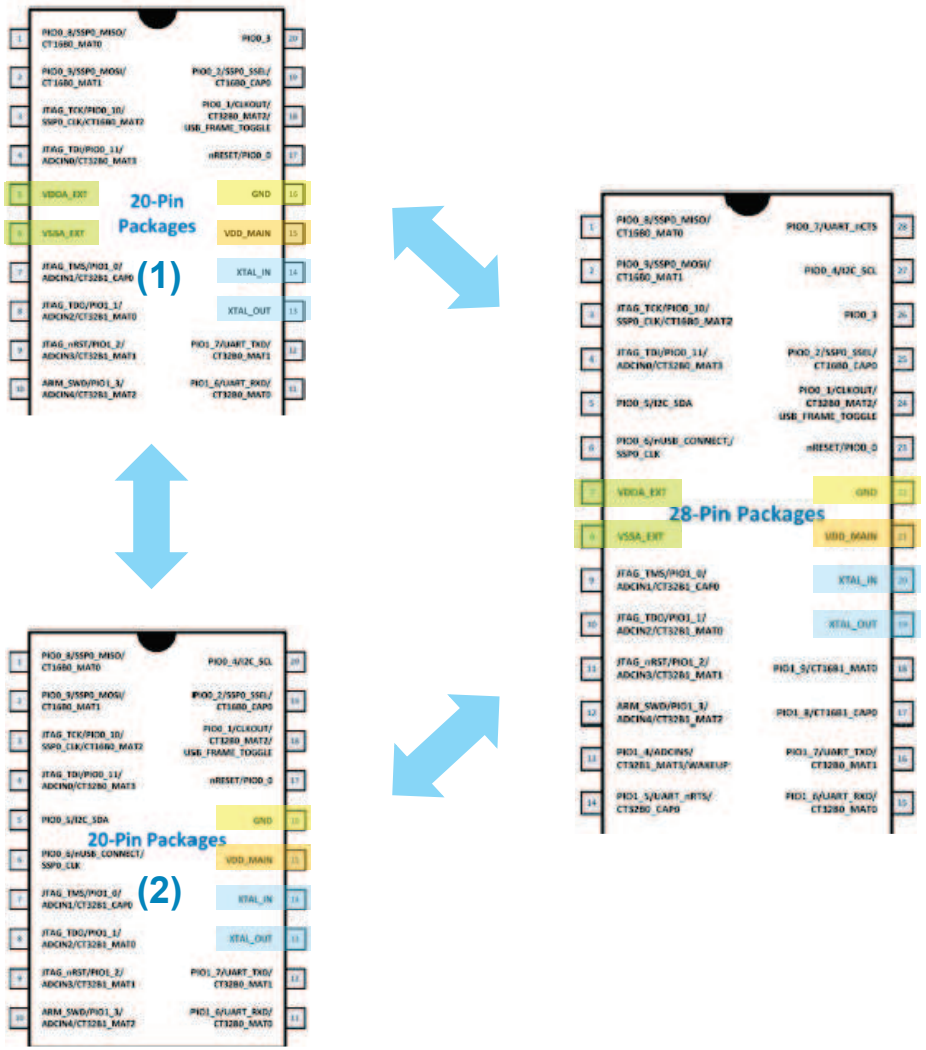
TSSOP20
(2 Options)

TSSOP28

DIP28

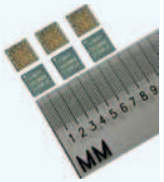
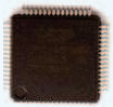
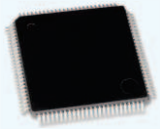
Final Part Number	SRAM	Flash	Package	Pin Count	I2C	SPI	UART	16b Timer	32b Timer	5CH-ADC	GPIO
LPC1110FD20	1	4	SO	20	1	1	1	2	2	1	16
LPC1111FDH20 /002	2	8	TSSOP	20	1	1	1	2	2	1	16
LPC1112FD20 /102	4	16	SO	20	1	1	1	2	2	1	16
LPC1112FDH20 /102	4	16	TSSOP	20	0	1	1	2	2	1	14
LPC1112FDH28 /102	4	16	TSSOP	28	1	1	1	2	2	1	22
LPC1114FDH28 /102	4	32	TSSOP	28	1	1	1	2	2	1	22
LPC1114FN28 /102	4	32	DIP	28	1	1	1	2	2	1	22

Designed for Scalability



- NXP's low-pin-count packages are designed for sharing system-critical pin-out
- Customers can easily swap or scale packages that fit their applications the most

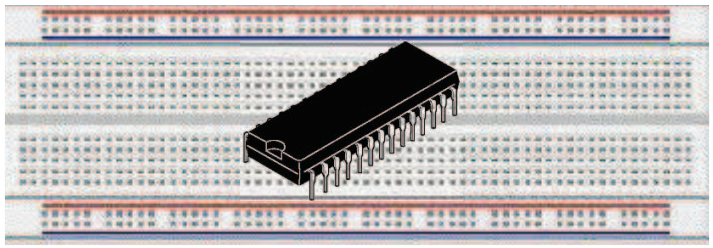
Widest Selection of Cortex-M0 Packages

Package	CSP16	QFN33	QFN33	QFP48	QFP64	QFP100	SO20	TSSOP20	TSSOP28	DIP28
Width (mm)	2	5	7	7	10	14	8	5	5	14
Length (mm)	2	5	7	7	10	14	13	7	10	35
Height (mm)	0.60	.85	.85	1.40	1.40	1.40	2.45	0.95	0.95	4.00
Sample Picture										

- NXP offers the widest selection of packages for Cortex-M0 devices
- World's smallest 32-bit ARM MCU – 2mm x 2mm
- World's first low-pin-count 32-bit ARM packages

Development Tools & Product Availability

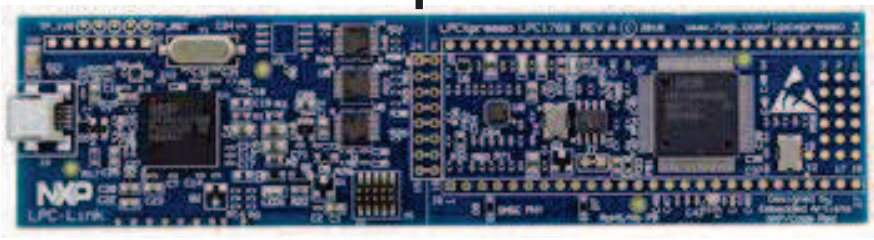
Breadboard



- Customer can develop prototype using DIP28 samples
- Existing IDE will support new packages

or

LPCXpresso



- Customer can develop prototype using LPCXpresso for LPC1100 (LPC1114)
- Then transfer code to the actual package