Si501/2/3

32 kHz–100 MHz CMEMS® Oscillator

Features

- Wide frequency range: 32 kHz to 100 MHz
  - Contact Silicon Labs for frequencies above 100 MHz
- Si501 single frequency w/ OE
- Si502 dual frequency w/ OE/FS
- Si503 quad frequency w/ FS
- ±20/30/50 ppm frequency stability including 10-year aging
- LVCMOS output
- Low period jitter
- Low power
- Continuous supply voltage range: +1.71 V to +3.63 V
- User selectable tRise/tFall options
- Glitchless start and stop
- Excellent short-term stability, long-term aging
- Industry standard footprints: 2x2.5, 2.5x3.2, 3.2x5 mm
- RoHS compliant, Pb-free
- Short lead times: <2 weeks
- –20 to +70 °C: Extnd commercial
- –40 to +85 °C: Industrial
- The Si50x family also includes Si504 for in-circuit programmability (See the Si504 Data Sheet)

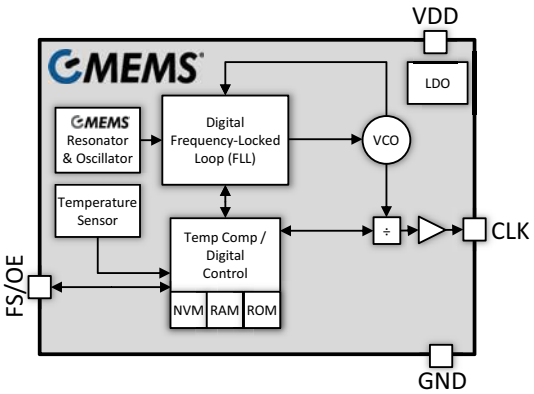
Applications

- Portable media players
- Digital cameras
- Digital camcorders
- Handheld gaming consoles
- Storage (SAS/SATA)
- Portable medical devices
- Office automation
- General purpose processors
- Embedded
- Industrial

Description

The Si501/2/3 CMEMS oscillator family provides monolithic, MEMS-based IC replacements for traditional crystal oscillators. Silicon Laboratories' CMEMS technology combines standard CMOS + MEMS in a single, monolithic IC to provide integrated, high-quality and high-reliability oscillators. Each device is factory tested and configured for guaranteed performance to data sheet specifications across voltage, process, temperature, shock, vibration, and aging. Additional information on the Si50x CMEMS oscillator architecture and CMEMS technology is available in white papers on the Silicon Labs website at www.silabs.com/cmems.

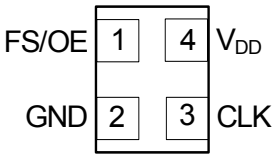
Functional Block Diagram



Ordering Information:

See Section 4.

Pin Assignments



Patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

V_{DD}=1.71 to 3.63 V, T_A= –40 to 85 °C, unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage[1]	V_{DD}		1.71	—	3.63	V
Supply Current	I_{DD1}	C_L=4 pF, 3.3 V_{DD}, F_{CLK}=1.0 MHz, low power option	—	1.7	2.5	mA
		C_L=4 pF, 3.3 V_{DD}, F_{CLK}=100 MHz, low power option	—	5.3	6.5	mA
		C_L=4 pF, 3.3 V_{DD}, F_{CLK}=1.0 MHz, low jitter option	—	3.9	4.9	mA
		C_L=4 pF, 3.3 V_{DD}, F_{CLK}=100 MHz, low jitter option	—	7.6	8.9	mA
Static Supply Current[2]	I_{DD2}	Mode=Stop[3], low power option Output disabled Internal oscillator F_{CLK}=1 MHz	—	1.7	2.5	mA
		Mode=Stop[3], low jitter option Output disabled Internal oscillator F_{CLK}=1 MHz	—	3.9	4.9	mA
		Mode=Doze[3, 4] Output disabled Oscillator in low power mode	—	670	890	µA
		Mode=Sleep[3, 5] Output disabled Oscillator turned off	—	0.3	1	µA
Input High Voltage	V_{IH}	FS/OE pin	0.70 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}	FS/OE pin	—	—	0.30 x V_{DD}	V
OE Internal Pull Resistor	R_I	Ordering option	—	50	—	kΩ
Operating Temperature	T_A	Extended commercial grade	–20	—	70	°C
		Industrial grade	–40	—	85	°C

Notes:

1. The supply voltage range is continuous from 1.71 to 3.63 V.
2. Si501 and Si502 only. Si503 has frequency select option only.
3. Si501 and Si502 only. Si503 has FS only and does not support Stop, Doze, or Sleep.
4. Si501, 3rd option code H, L. Si502, 3rd option code E.
5. Si501, 3rd option code J, M. Si502, 3rd option code F.

Table 2. Output Clock Characteristics

V_{DD}=1.71 to 3.63 V, T_A= –40 to 85 °C, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Range	F_{CLK}		0.032	—	100	MHz
Clock Period	T_{CLK}	$1/F_{CLK}$	31,250	—	10	ns
Total Stability[1]	F_{STAB}		–20	—	+20	ppm
			–30	—	+30	ppm
			–50	—	+50	ppm
Initial Accuracy	F_I	Measured at 25 °C at the time of shipping	—	±2	—	ppm
Startup Time[2]	T_{SU}	From V_{DD} crossing 1.71 V to first clock output	—	2.5	4	ms
Resume Time[3,4]	T_{RUN}	From Sleep mode	—	2	5	ms
		From Doze mode	—	1.7	2.55	ms
		From Stop mode[5]	—	—	1.5 x T_{CLK} + 35	ns
Output Disable Time[3,4]	T_D	To Sleep/Doze mode, from output running	—	—	225	µs
		To Stop, from output running	—	—	1.5 x T_{CLK} + 35	ns
Frequency Update Time[4,6]	T_{NEW_FREQ}		—	—	5	ms

Notes:

1. Orderable option. Stability budget consists of initial tolerance, operating temperature range, rated power supply voltage change, load change, aging, shock, and vibration.
2. Hold FS/OE high (strong or weak) during powerup for fastest time to clock.
3. Si501 and Si502 only. Si503 has FS only and does not support Stop, Doze, or Sleep.
4. Asserted FS/OE actions must be held stable for the maximum duration of the invoked FS/OE event (e.g., T_{RUN}, T_{NEW_FREQ}, T_D, etc).
5. If the Si502 frequency is switched while the device is in Stop mode, the frequency prior to Stop will be output briefly until the glitchless switch to the other frequency. Doze mode does not have this behavior.
6. Si502 and Si503 only. Si501 is a single frequency device with OE only.

Table 3. Output Clock Levels and Symmetry

V_{DD} = 1.71 to 3.63 V, T_A = –40 to 85 °C unless otherwise indicated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage	V_{OH}	1st ordering option code: A and H I_{OH}=–4 mA	0.90 x V_{DD}	—	—	V
Output Low Voltage	V_{OL}	1st ordering option code: A and H I_{OH}=+4 mA	—	—	0.10 x V_{DD}	V
Rise/Fall Time[1]	tRise /tFall	1st ordering option code: A and H	0.4	0.7[2]	1.2	ns
		1st ordering option code: B and J Z_0= 50 Ω @ 1.8V	1	1.3	1.6	ns
		1st ordering option code: C and K Z_0= 50 Ω @ 2.5V	1	1.3	1.6	ns
		1st ordering option code: D and L Z_0 = 50 Ω @ 3.3V	1	1.3	1.6	ns
		1st ordering option code: E and M	2	3	4	ns
		1st ordering option code: F and N	4	5	7	ns
		1st ordering option code: G and P	7	8	11	ns
Duty Cycle	DC	Drive strength selected such that tRise/tFall (20% to 80%)<10% of period	45	50	55	%

Notes:
1. C_L=15 pF, tRise/tFall (20% to 80%), 3.3 V, unless otherwise stated.
2. Recommended series termination resistor = 24.9 to 27.4 Ω for Z_0=50 Ω.

Table 4. Output Clock Jitter and Phase Noise

V_{DD} = 1.71 to 3.63 V, T_A = –40 to 85 °C unless otherwise indicated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle-to-Cycle Jitter	J_{CCPP}	100 MHz, Low Jitter Option 1st ordering option code: H	—	14	25	ps pk-pk
		100 MHz, Low Power Option 1st ordering option code: A	—	16	26	ps pk-pk
Period Jitter	J_{PRMS}	100 MHz, Low Jitter Option 1st ordering option code: H	—	1	1.6	ps rms
		100 MHz, Low Power Option 1st ordering option code: A	—	1.3	1.9	ps rms
Period Jitter Pk-Pk	J_{PPKPK}	Low Jitter Option 10k samples 1st ordering option code: H	—	9	13	ps pk-pk
		Low Power Option 10k samples 1st ordering option code: A	—	10	16	ps pk-pk
Phase Jitter[1]	ϕ	75 MHz F_{OFFSET}=900 kHz to 7.5 MHz Low Jitter Option 1st ordering option code: H	—	1	1.3	ps rms
		75 MHz F_{OFFSET}=900 kHz to 7.5 MHz Low Power Option 1st ordering option code: A	—	2.5	3.2	ps rms

Notes:

1. Integrated phase jitter exceeds the requirements of some high-performance data communications systems. See AN783 for additional information.

Table 5. Environmental Compliance and Package Information

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Temperature Cycle	JESD22, Method A104
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level (MSL)	2
Contact Pads	Gold over Nickel/Palladium

Table 6. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Impedance	θ_{JA}	3.2x5 mm, still air	187	°C/W
		2.5x3.2 mm, still air	239	
		2x2.5 mm, still air	241	

Table 7. Absolute Maximum Limits[1]

Parameter	Symbol	Rating	Unit
Maximum Operating Temperature	T_{MAX}	85	°C
Storage Temperature	T_S	–55 to +125	°C
Supply Voltage	V_{DD}	–0.5 to +3.8	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.3V	V
ESD Sensitivity (JESD22-A114)	HBM	2000	V
ESD Sensitivity (CDM)	CDM	500	V
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	°C
Soldering Time at T_{PEAK} (PB-free profile)[2]	T_P	20–40	s
Junction Temperature	T_J	125	°C

Notes:
1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

2. Si50x Typical Applications Circuits, AC Waveforms, and Functional Descriptions

The Si50x family has various applications circuits and ac waveforms depending on the selected device and ordering configuration options. Pay careful attention when reading the following section to be sure you refer to the correct diagrams.

2.1. Si501/2 Applications Circuits

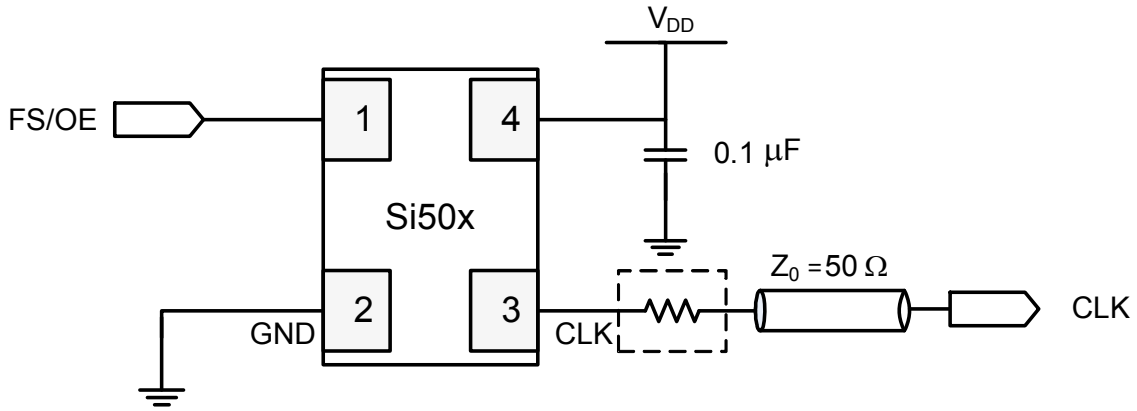
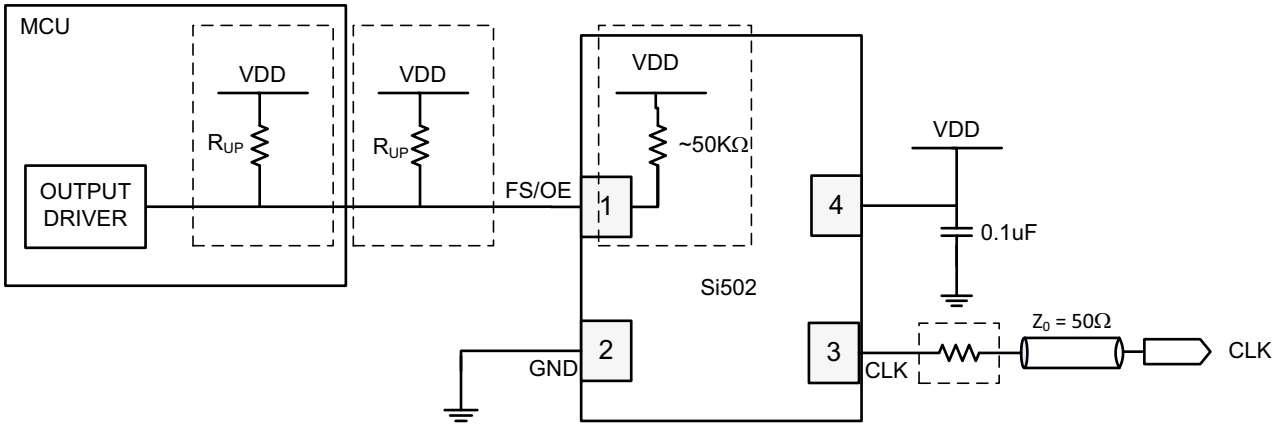


Figure 1. Si50x Applications Circuit with Optional Output Series Resistor

Note: The dotted line box in Figure 1 is an optional component depending on tRise/tFall configuration option. This diagram applies to all Si50x product drive strength configuration options. See Ordering Guide for detail.



Note: The dotted line boxes in Figure 2 show resistor options depending on MCU pull-up resistors configuration and the Si50x internal resistor configuration options. See Ordering Guide for Si50x configuration option details. Users should design only one of the pin 1 dotted-line options. The series resistor on pin 3 is also optional.

Figure 2. Si502 Applications Circuit with Configuration Options

Table 8. Si502 FS/OE States and Resistor Values

FS/OE Pin State	R_{UP}	Clock Output
Strong High	$0\ \Omega \le R_{UP} \le 1\ k\Omega$	Frequency 1
Weak High	$20\ k\Omega \le R_{UP} \le 200\ k\Omega$	Frequency 2
Low	—	Hi-Z

Notes:
1. If the Si502 internal pull-up resistor configuration option is not selected, an MCU internal pull-up resistor or an external pull-up resistor should be used.
2. The parallel combination of all pull-up resistors on the FS/OE pin, including the optional internal device pull-up resistor must be > 20 kΩ to select the Weak High state.
3. If the Si50x internal pull-up resistor is enabled with no other external OE connections, the OE state will be detected as `Weak High' which selects the Frequency 2 output by default.

2.2. Si501/2 AC Waveforms and Functional Descriptions

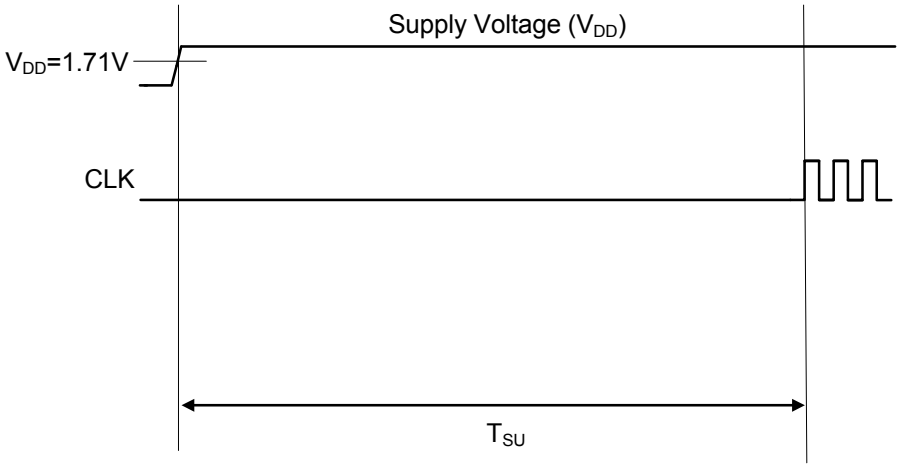


Figure 3. Si501/2 Power On Time (refer to Table 2)

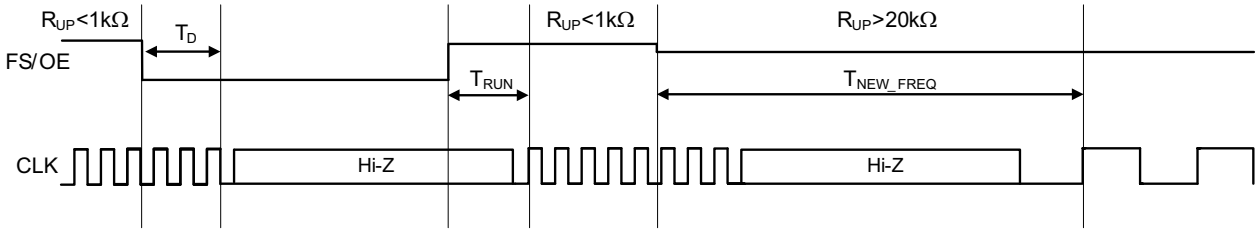
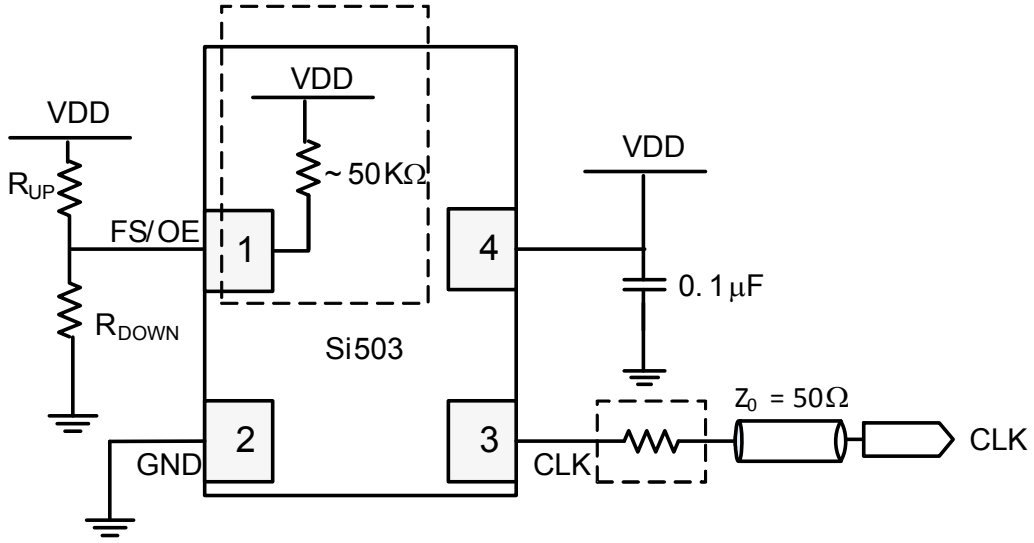


Figure 4. Si501/2 AC Waveform (refer to Table 2)

2.3. Si503 Applications Circuits

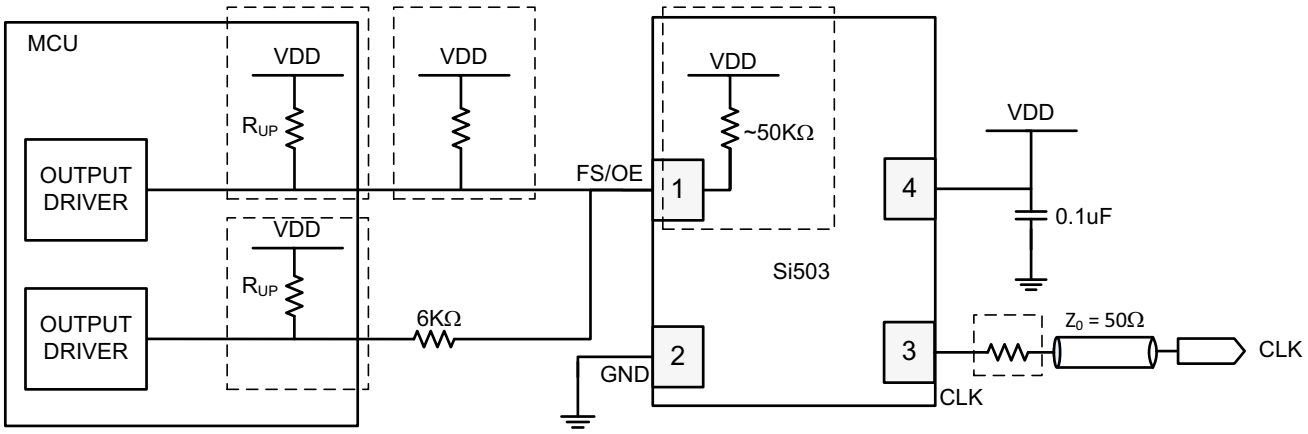


Note: The dotted line boxes show optional components depending on tRise/tFall and internal pull up resistor configuration options. See Ordering Guide for details.

Figure 5. Si503 Applications Circuit with Configuration Options

Table 9. Si503 Frequency Select with External Resistor Options

FS/OE Pin State	R_{UP}	R_{DOWN}	Clock Output
Strong High	$0\ \Omega \le R_{UP} \le 1\ k\Omega$	Do not populate	Frequency 1
Weak High	$20\ k\Omega \le R_{UP} \le 200\ k\Omega$	Do not populate	Frequency 2
Weak Low	Do not populate	$20\ k\Omega \le R_{DOWN} \le 200\ k\Omega$	Frequency 3
Strong Low	Do not populate	$0\ \Omega \le R_{DOWN} \le 1\ k\Omega$	Frequency 4
Note: If the Si50x internal pull-up resistor is enabled with no other external OE connections, the OE state will be detected as `Weak High' which selects the Frequency 2 output by default.			



Note: The dotted line boxes in Figure 6 show resistor options depending on MCU pull-up resistors configuration and the Si503 internal resistor configuration options. See Ordering Guide for configuration option details. Users should design only one of the pin 1 dotted-line options. The series resistor on pin 3 is also optional.

Figure 6. Si503 Applications Circuit with MCU and Configuration Options

Table 10. Si503 Frequency Select

FS/OE Pin State	MCU Output 1	MCU Output 2	Clock Output
Strong High	High	Hi-Z	Frequency 1
Weak High	Hi-Z	Hi-Z	Frequency 2
Weak Low	Hi-Z	Low	Frequency 3
Strong Low	Low	Hi-Z	Frequency 4
Note: If the Si50x internal pull-up resistor is enabled with no other external OE connections, the OE state will be detected as `Weak High' which selects the Frequency 2 output by default.			

2.4. Si503 AC Waveform and Functional Description

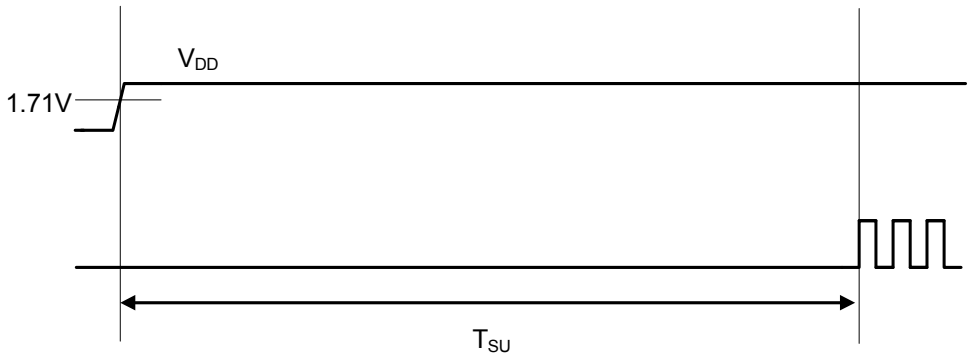


Figure 7. Si503 Power On Time (refer to Table 2)

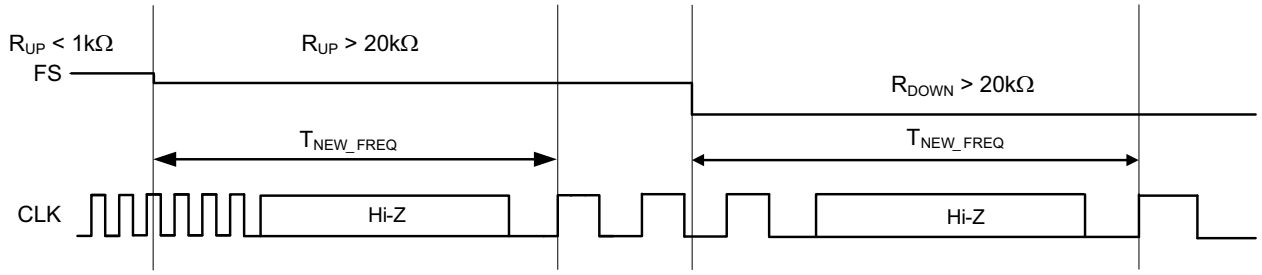


Figure 8. Si503 AC Waveform (refer to Table 2)

3. Pin Descriptions

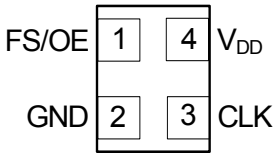


Figure 9. Si501/2/3

Table 11. Pin Description

Pin	Name	Function
1	FS/OE	FS=Frequency Select. Si502 and Si503 only. OE=Output Enable. Si501 and Si502 only.
2	GND	Ground.
3	CLK	Output clock.
4	V_{DD}	Power supply. Bypass with a 0.1μF capacitor placed as close to the V_{DD} pin as possible.

4. Ordering Guide

The Si50x family of CMEMS oscillators are highly configurable. Each orderable part number must be specified according to the guidelines below. Each customized part's performance is guaranteed to operate within the data sheet specifications. An on-line configuration and ordering tool is available at www.silabs.com/cmems.

4.1. Si501 Ordering Guide and Part Number Syntax

501	X	X	X	XXXXXXX	X	A	X	R

1st Option Code — VDD, Jitter/Power, tRise/tFall

	VDD	Jitter vs Power	TYP T_R/T_F
A	ALL	Lower Power[1]	0.7ns
B	3.3V	Lower Power[2]	1.3ns
C	2.5V	Lower Power[2]	1.3ns
D	1.8V	Lower Power[2]	1.3ns
E	ALL	Lower Power[3]	3ns
F	ALL	Lower Power[3]	5ns
G	ALL	Lower Power[3]	8ns
H	ALL	Lower Jitter[1]	0.7ns
J	3.3V	Lower Jitter[2]	1.3ns
K	2.5V	Lower Jitter[2]	1.3ns
L	1.8V	Lower Jitter[2]	1.3ns
M	ALL	Lower Jitter[3]	3ns
N	ALL	Lower Jitter[3]	5ns
P	ALL	Lower Jitter[3]	8ns

2nd Option Code — Freq Stability

	ppm
A	± 50
B	± 30
C	± 20

3rd Option Code — Output Enable

	OE High	OE Low	Internal Pull Resistor
A	Enable	Stop	Pull-Up
B	Enable	Doze	Pull-Up
C	Enable	Sleep	Pull-Up
D	Stop	Enable	Pull-Down
E	Doze	Enable	Pull-Down
F	Sleep	Enable	Pull-Down
G	Enable	Stop	None
H	Enable	Doze	None
J	Enable	Sleep	None
K	Stop	Enable	None
L	Doze	Enable	None
M	Sleep	Enable	None

Frequency Code

Freq.	Description
Mxxxxxx	f_{OUT} < 1 MHz
xMxxxxx	1 MHz ≤ f_{OUT} < 10 MHz
xxMxxxx	10 MHz ≤ f_{OUT} < 100 MHz
100M000	f_{OUT} = 100 MHz
xxxxxx	SiLabs-generated 6-digit custom code if required frequency is > 6 decimal resolution.

Package Dimension

	Dimension
B	3.2 x 5 mm[5]
C	2.5 x 3.2 mm
D	2 x 2.5 mm

Die Revision

Revision
A

Temp Range

	Range
F	-20 to 70 C
G	-40 to 85 C

Tape & Reel Option

	Option
R	Reel
	Tape

Notes:
1. Series termination resistor is recommended for this configuration. See Table 4 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Output impedance is 50Ω for the indicated supply condition. Reduced EMI setting.
4. Example of Si501 orderable part number with 10 MHz output frequency: 501ACA10M000BAF.
5. Silabs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.

Figure 10. Si501 Part Number Syntax

4.2. Si502 Ordering Guide and Part Number Syntax

502	X	X	X	XXXXXX	X	A	X	R

1st Option Code — VDD, Jitter/Power, tRise/tFall

	VDD	Jitter vs Power	TYP T_R/T_F
A	ALL	Lower Power[1]	0.7ns
B	3.3V	Lower Power[2]	1.3ns
C	2.5V	Lower Power[2]	1.3ns
D	1.8V	Lower Power[2]	1.3ns
E	ALL	Lower Power[3]	3ns
F	ALL	Lower Power[3]	5ns
G	ALL	Lower Power[3]	8ns
H	ALL	Lower Jitter[1]	0.7ns
J	3.3V	Lower Jitter[2]	1.3ns
K	2.5V	Lower Jitter[2]	1.3ns
L	1.8V	Lower Jitter[2]	1.3ns
M	ALL	Lower Jitter[3]	3ns
N	ALL	Lower Jitter[3]	5ns
P	ALL	Lower Jitter[3]	8ns

2nd Option — Freq Stability

	ppm
A	± 50
B	± 30
C	± 20

3rd Option Code — FS / OE[6]

	OE Low	Internal Pull Resistor
A	Stop	Pull-Up
B	Doze	Pull-Up
C	Sleep	Pull-Up
D	Stop	None
E	Doze	None
F	Sleep	None

Frequency Code

Freq.	Description
xxxxxx	SiLabs-generated 6-digit custom code.

Package Dimension

	Dimension
B	3.2 x 5 mm[5]
C	2.5 x 3.2 mm
D	2 x 2.5 mm

Die Revision

Revision
A

Temp Range

	Range
F	-20 to 70 C
G	-40 to 85 C

Tape & Reel Option

	Option
R	Reel
	Tape

Notes:
1. Series termination resistor is recommended for this configuration. See Table 4 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Output impedance is 50Ω for the indicated supply condition. Reduced EMI setting.
4. Example of Si502 orderable part number: 502ACA123456BAF.
5. Silabs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.
6. The Si502 OE pin has three (3) states: OE High = Freq 1; OE Weak High = Freq 2; OE Low is configurable.

Figure 11. Si502 Part Number Syntax

4.3. Si503 Ordering Guide and Part Number Syntax

503	X	X	X	XXXXXX	X	A	X	R

1st Option Code — VDD, Jitter/Power, tRise/tFall

	VDD	Jitter vs Power	TYP T_R/T_F
A	ALL	Lower Power[1]	0.7ns
B	3.3V	Lower Power[2]	1.3ns
C	2.5V	Lower Power[2]	1.3ns
D	1.8V	Lower Power[2]	1.3ns
E	ALL	Lower Power[3]	3ns
F	ALL	Lower Power[3]	5ns
G	ALL	Lower Power[3]	8ns
H	ALL	Lower Jitter[1]	0.7ns
J	3.3V	Lower Jitter[2]	1.3ns
K	2.5V	Lower Jitter[2]	1.3ns
L	1.8V	Lower Jitter[2]	1.3ns
M	ALL	Lower Jitter[3]	3ns
N	ALL	Lower Jitter[3]	5ns
P	ALL	Lower Jitter[3]	8ns

2nd Option Freq Stability

	ppm
A	± 50
B	± 30
C	± 20

3rd Option Code Output Enable

	Internal Pull Resistor
A	Pull-Up
B	None

Frequency Code

Freq.	Description
xxxxxx	SiLabs-generated 6-digit custom code.

Package Dimension

	Dimension
B	3.2 x 5 mm[5]
C	2.5 x 3.2 mm
D	2 x 2.5 mm

Die Revision

Revision
A

Temp Range

	Range
F	-20 to 70 C
G	-40 to 85 C

Tape & Reel Option

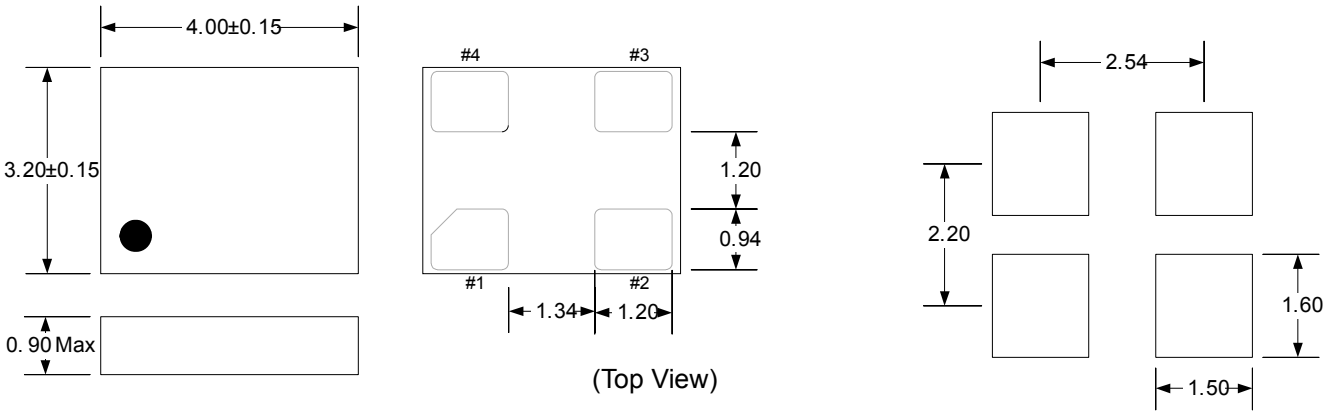
	Option
R	Reel
	Tape

Notes:
1. Series termination resistor is recommended for this configuration. See Table 4 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Output impedance is 50Ω for the indicated supply condition. Reduced EMI setting.
4. Example of Si503 orderable part number: 503ACA123456BAF.
5. Silabs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.

Figure 12. Si503 Part Number Syntax

5. Package Dimensions and Land Patterns

5.1. Package Outline: 3.2 x 5 mm 4-pin DFN



Note: The 3.2 x 5 mm package is delivered as a 3.2 x 4 mm package and is drop-in compatible to industry-standard 3.2 x 5 landing patterns.

Figure 13. 3.2 x 5 mm 4-pin DFN

5.2. Package Outline: 2.5 x 3.2 mm 4-pin DFN

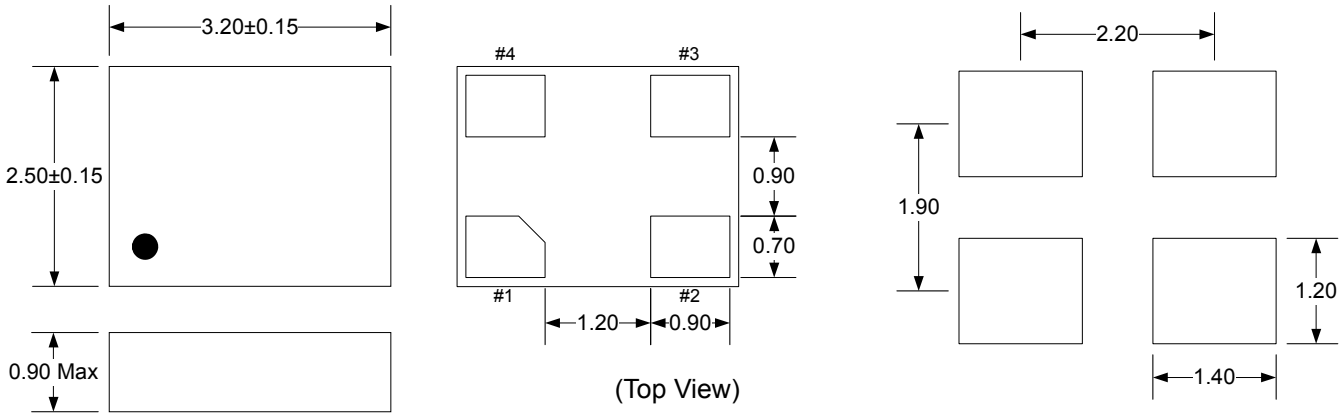


Figure 14. 2.5 x 3.2 mm 4-pin DFN

5.3. Package Outline: 2 x 2.5 mm 4-pin DFN

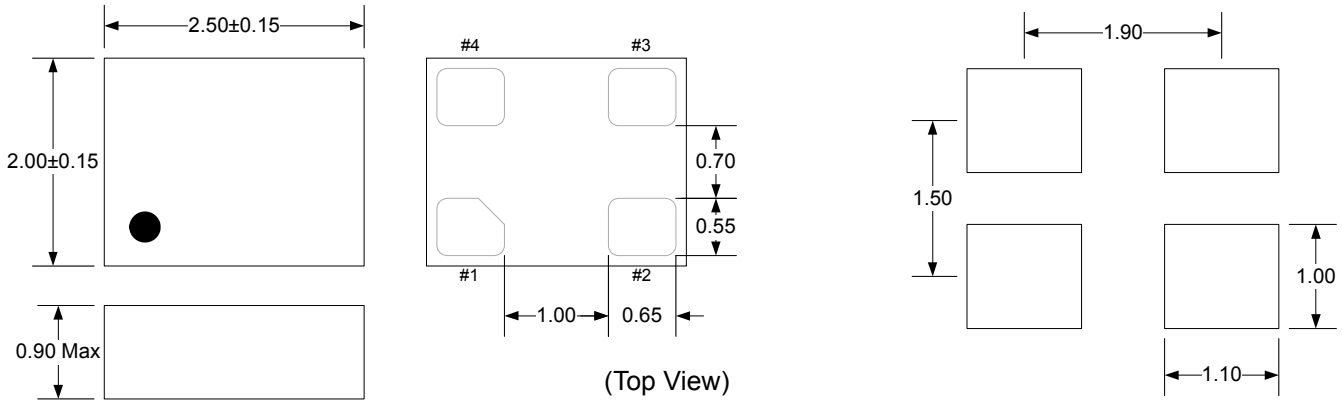
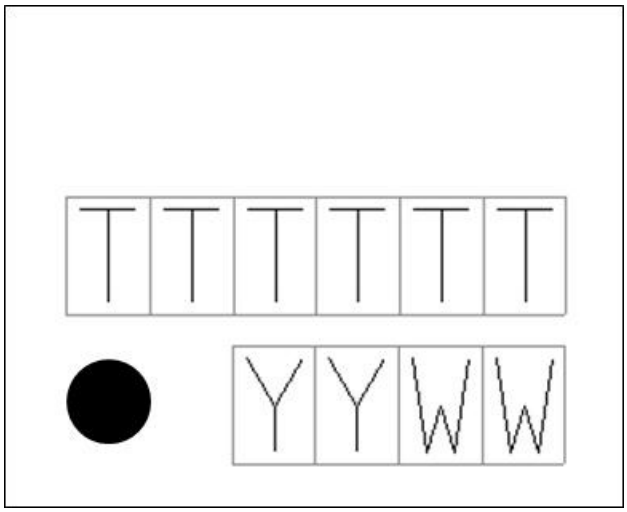


Figure 15. 2 x 2.5 mm 4-pin DFN

6. Top Markings

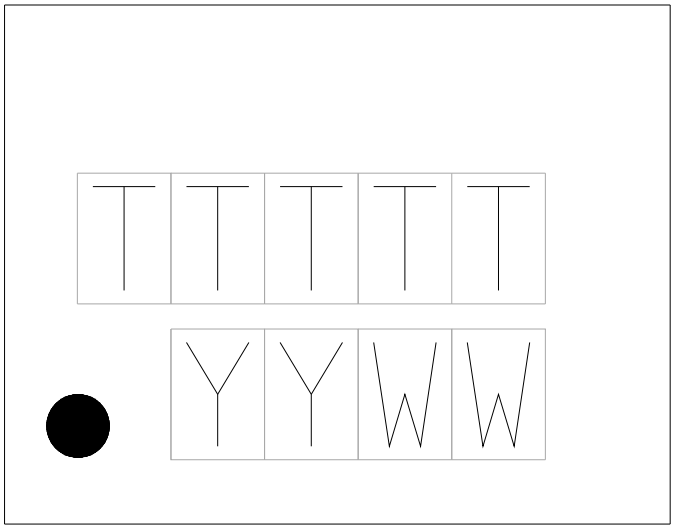
6.1. 3.2 x 5 mm Top Marking



6.2. 3.2 x 5 mm Top Marking Explanation

Mark Method:	Laser	
Font Size:	0.60 mm Right-Justified	
Line 1 Marking:	TTTTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
Line 2 Marking	Circle=0.5 mm Diameter Left-Justified	Pin 1 Indicator
	YY=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

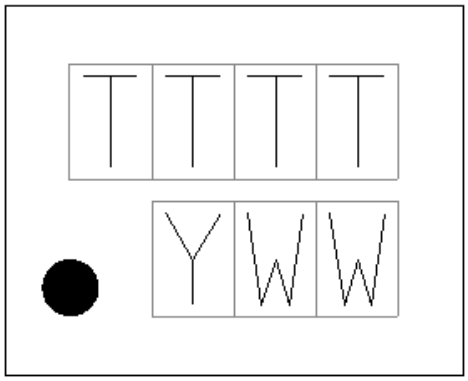
6.3. 2.5 x 3.2 mm Top Marking



6.4. 2.5 x 3.2 mm Top Marking Explanation

Mark Method:	Laser	
Font Size:	0.50 mm Right-Justified	
Line 1 Marking:	TTTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
Line 2 Marking:	Circle=0.3 mm Diameter Left-Justified	Pin 1 Indicator
	Y=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

6.5. 2 x 2.5 mm Top Marking



6.6. 2 x 2.5 mm Top Marking Explanation

Mark Method:	Laser	
Font Size:	0.50 mm Right-Justified	
Line 1 Marking:	TTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
Line 2 Marking:	Circle=0.3 mm Diameter Left-Justified	Pin 1 Indicator
	Y=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

Document Change List

Revision 0.2 to Revision 0.3

- Combined Si501/2/3 data sheets.
- Modified title page.
- Modified Table 2.
- Modified Table 4.
- Modified Section 2.
- Modified Section 3.
- Modified Section 4.
- Modified Section 5.

Revision 0.3 to Revision 0.4

- Modified title page.
- Modified Table 1.
- Modified Table 2.
- Modified Table 3.
- Modified Table 4.
- Modified Table 5.
- Modified Table 6.
- Modified Table 7.
- Modified Section 2.
- Modified Section 4.
- Modified Section 5.
- Modified Section 6.

Revision 0.4 to Revision 0.41

- Modified Table 4.

Revision 0.41 to Revision 0.7

- Revised supported frequency range.
- Added MIN/MAX figures to all relevant tables.

Revision 0.7 to Revision 0.71

- Revised Table 3.
- Revised Section 5.

NOTES:

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