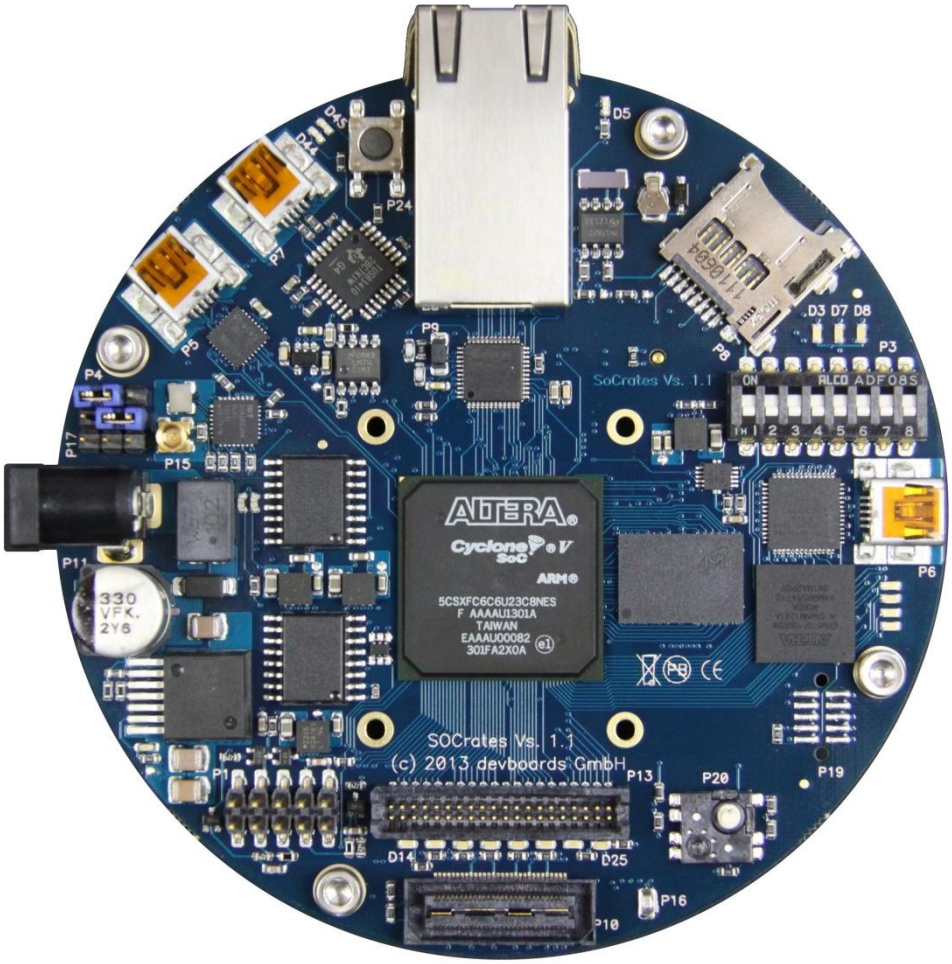
Datasheet

SoCrates

Cyclone V SoC Evaluation Board



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Contents

Revisions

Document Revision

Revision	Remark	Date
1.00	Initial Version	08.04.2013
1.2	Added SoCrates-Phy1 Board	20.06.2013

Hardware Revisions

Revision	Remark	Date
1.0	Initial Version	15.02.2013
1.1	Error Fixing : • JTAG order of device changed • BSEL1 on wrong signal • DDR3 Termination added • Ethernet Phy adapted from PEF7072 to PEF7071 • BSEL jumper added for boot from SDCard or QSPI Flash	08.04.2013
1.3	Added Jumper for MSEL Error Fixing: • RJ45 Connector Pin Swap	16.06.2013

Ordering Information

SoCrates

- SoCrates Evaluation Board
- 90 - 240V wall power supply
- Two Mini-USB cables
- Micro SDCard with Linux Image

SoCrates-Phy1

- Dual Ethernet Phy add-on board with Access-IP Key

Introduction

SoCrates is one of the first evaluations Boards based on Altera Cyclone V SoC devices. The board provides the IO signals of a selected set of peripherals of the SoC-Part and also from the FPGA-Part of the HPS (Hard-Processor-System). These IOs are available at different connectors of the board. An embedded USB-Blaster II allows the communication with the internal JTAG interfaces of the SoC device. The configuration of the device can be done in several different ways. One method is to configure the FPGA-Part via a QSPI Flash, while the HPS can boot from either QSPI, SDCard or NAND interface. The SoCrates board provides 1 Gbyte 32 bit DDR3 Memory running at 400MHz used to hold the operating system.

As Altera delivers currently only engineering samples of SGX devices, the first boards will be equipped with 5CSXFC6C6U23C8NES devices. They are pin-to-pin compatible with the 5CSEBA6U23C8N devices which will be finally used. The transceivers are not used on the board.

- 5CSEBA6U23C8
- EPCQ256 configuration device
- EPCQ266 Boot device
- 1GByte x32 DDR3 Memory
- PEF7071 Gigabit Ethernet Phy
- USB 2.0 OTG Phy
- UART / USB Converter
- CAN Driver
- LM74 I²C temperature sensor
- RTC with Goldcap
- 16 GPIO 3.3V (HPS)
- 3 User LEDs
- 8-DIP-Switch

- 30 GPIO 3.3V
- 32 GPIO 2.5 / 3.3V

- LVDS Interface on High-Speed Connector
- LVDS TFT Interface (4.Lanes)+ four 3.3V GPIOs
- 8x User LEDs
- Navigation key
- JTAG interface
- Embedded ΣΔ-ADC /DAC

- Embedded USB-Blaster II

- on board 5V, 3.3V, 2.5V, 1.5V and 1.1V power supply

- dimension : 100mm diameter

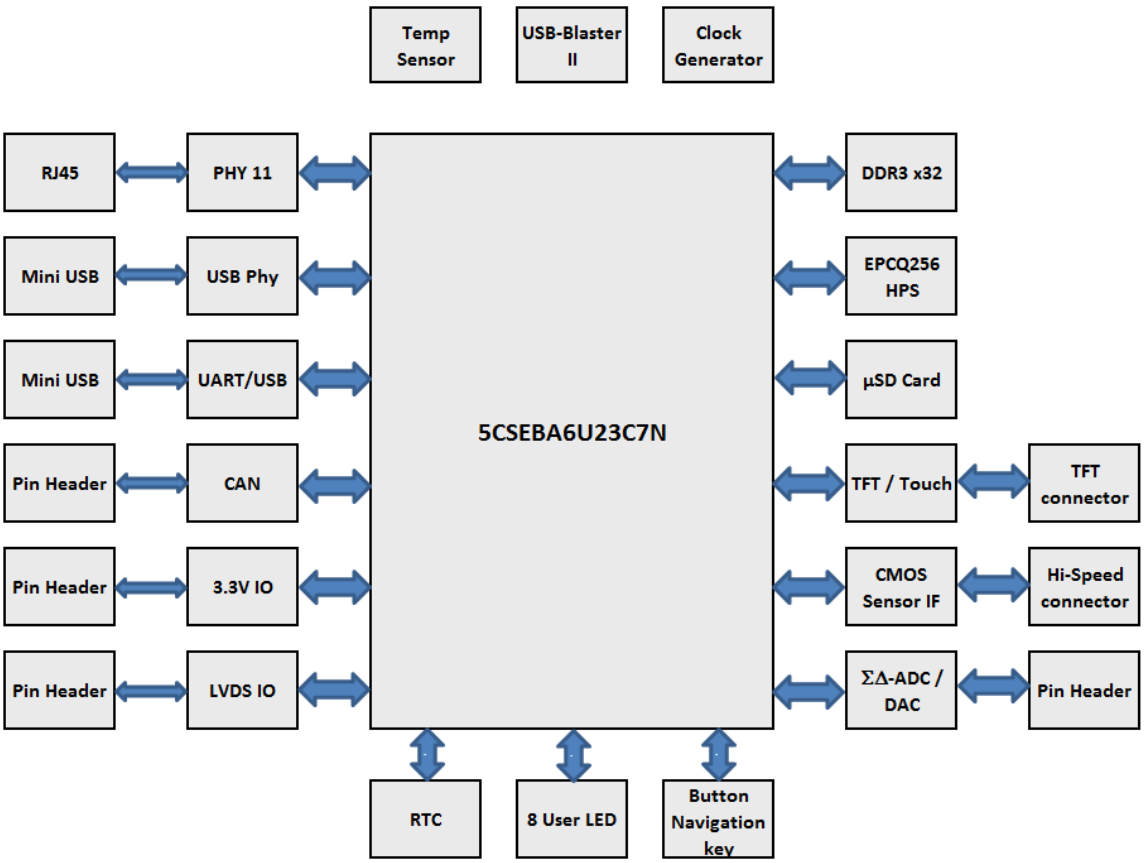

Temp Sensor
USB-Blaster II
Clock Generator
RJ45
PHY 11
Mini USB
USB Phy
Mini USB
UART/USB
Pin Header
CAN
Pin Header
3.3V IO
Pin Header
LVDS IO
5CSEBA6U23C7N
DDR3 x32
EPCQ256 HPS
µSD Card
TFT / Touch
TFT connector
CMOS Sensor IF
Hi-Speed connector
ΣΔ-ADC / DAC
Pin Header
RTC
8 User LED
Button Navigation key

Figure 1

Pin-Header Locations (top side)

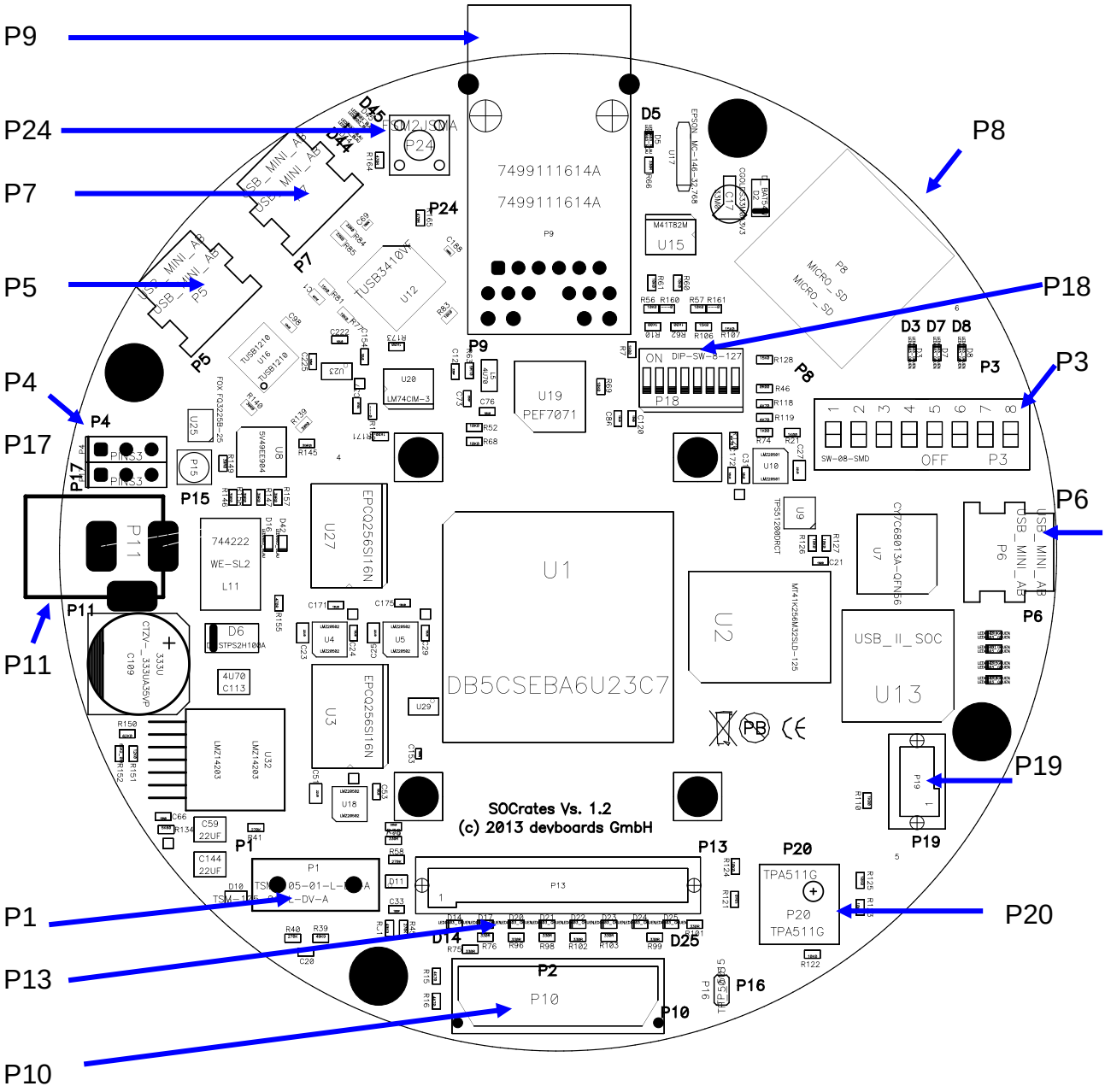


Figure 2I

Pin-Header Locations (bottom side)

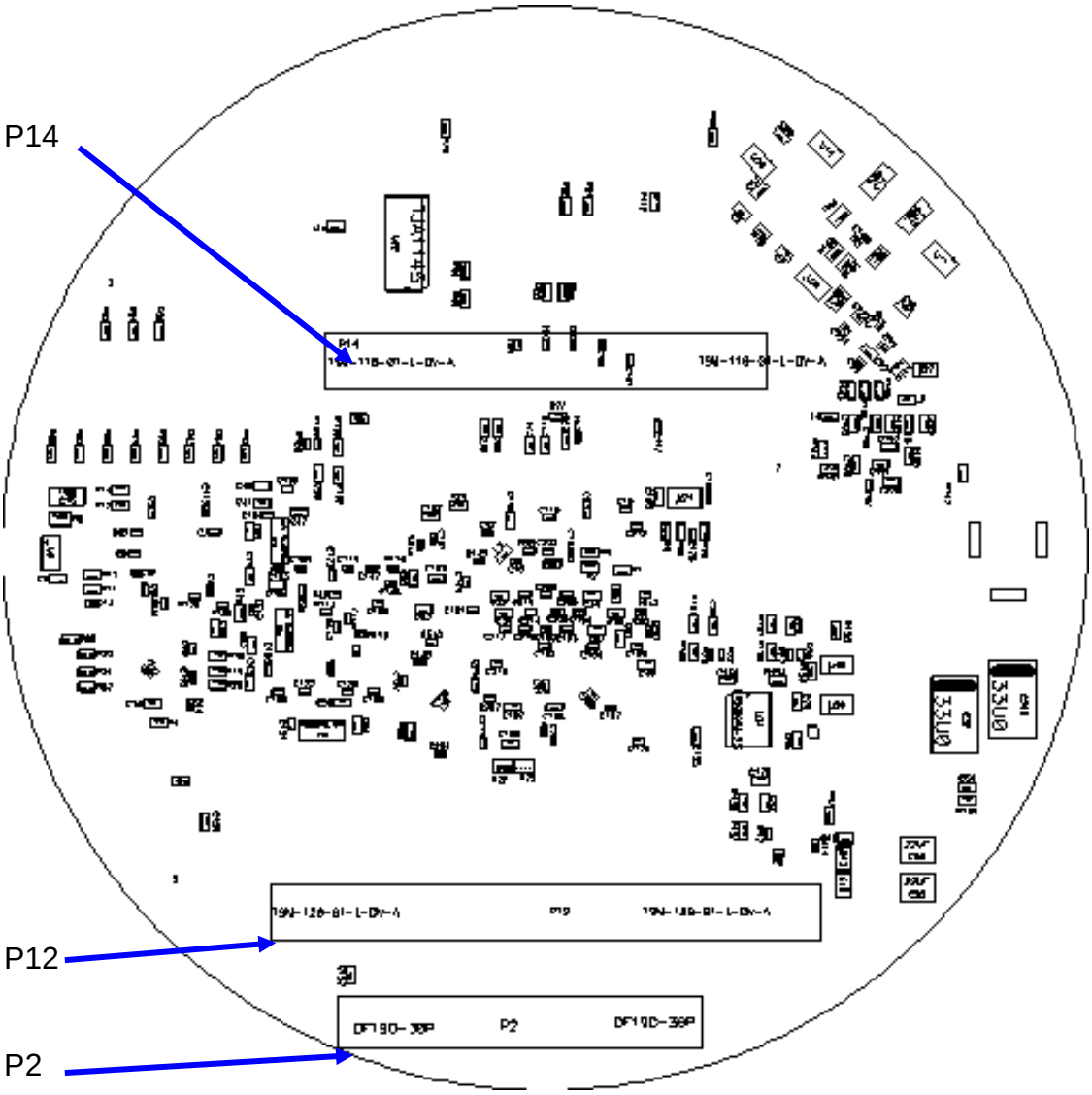


Figure 3

Installation

For installation of the documentation, the applications and the reference designs please download the "SoCrates_setup.exe" file which is available at the www.devboards.de/download website for download. After starting the setup program the files will be installed on your hard disk as shown below.

The reference designs are build with Quartus II version 13.0. You can download the complete set of Altera design software and tools from the Altera website: software.altera.com

Please install the applications in the following sequence:

- install the Quartus® 13.0 Full Edition or Web Edition
- install the Embedded Software 13.0
- install the SoCrates reference designs.

Getting started

Documentation

The complete documentation of the board, the reference designs, IP functions and the onboard devices are stored in the documentation directory of the Altera® Nios®II directory e.g. C:\Altera\13.0\kits\SoCrates\documents

Setting up the board for Linux

1) Check the jumper of the board. For default setting the jumper P4 should connect Pin 1 and 2.
2) Set the Dip Switch (1.27mm Grid) P18 to
   OFF OFF ON ON OFF ON OFF ON
   This selects FPGA boot mode Active Serial and SDCard as boot source for the HPS.
3) Insert the SDCard with a Linux Image into the SDCard slot.
4) Connect the UART with a mini-USB Cable between connector (P7) and your PC.
5) Power up the board
6) Check that the USB/UART device driver is loaded and the respective UART is available. If no driver is installed by default, you can find the driver for the TUSB3410 device in the driver subfolder.
7) Open a terminal program for the respective UART, setup the baudrate to 57600 and press the reset button on the board. (P24)
8) Your terminal should display the Linux Boot-Sequence now.

Setting up the board for JTAG

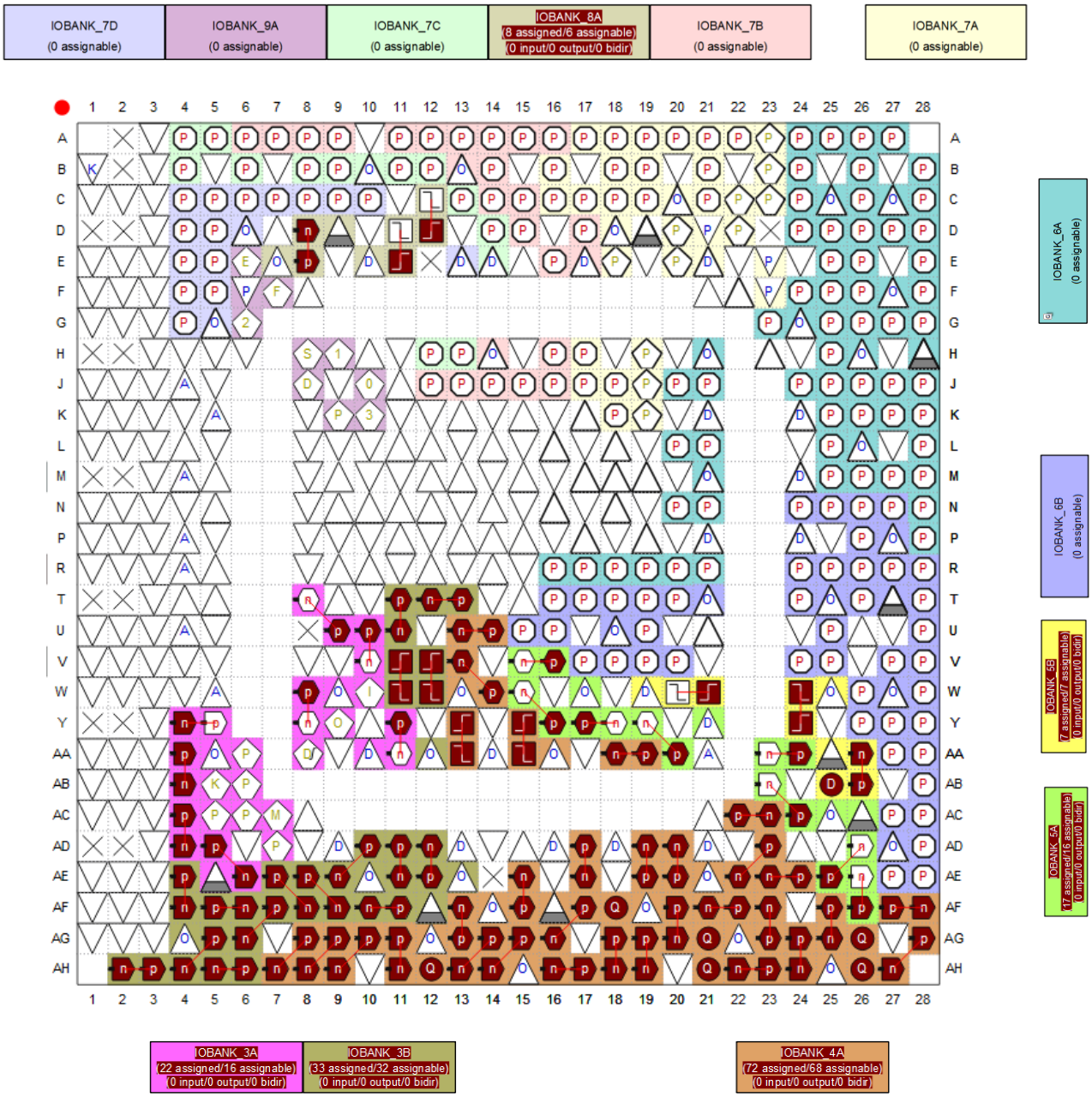
1) Check the jumper of the board. For default setting the jumper P4 should connect Pin 1 and 2.
2) Set the Dip Switch (1.27mm Grid) P18 to
   OFF OFF ON ON OFF ON OFF ON
   This selects FPGA boot mode Active Serial and SDCard as boot source for the HPS.
1) Connect the USB cable between the USB-Blaster II (P6) and your PC.
2) Power up the board.
3) The USB-Blaster II should be recognized as JTAG-Cable in the "Device Manager".
4) Now you can start Quartus II and work with the board

Reference designs

- Tbd

Board Description

FPGA IO-Banks



IO-Bank	Voltage	VCCPD	VREF
3A	2.5V	2.5V	
3B	3.3V	3.3V	
4A	3.3V	3.3V	
5A	2.5V	2.5V	
5B	2.5V	2.5V	
6A	1.35V	2.5V	0.675V
6B	1.35V	2.5V	0.675V
7A	3.3V	3.3V	
7B	3.3V	3.3V	
7C	3.3V	3.3V	
7D	1.8V	2.5V	
8A	2.5V	2.5V	

Table 1

FPGA Configuration

The SoCrates board provides an embedded USB-Blaster II and a QSPI Flash to configure the FPGA. Additionally the FPGA can be configured from the HPS. The QSPI Flash can be programmed using the JTAG indirect configuration (.jic) files. The .jic file can be generated in the Quartus®II software. The according dialog can be found in the Quartus II menu: File / Convert Programming Files.

FPGA Configuration select with MSEL (P18)

The MSEL pins are connected to the DIP-Switch P18. These signals are used to select the configuration scheme of the FPGA. SoCrates supports configuration via the QSPI Flash or the HPS processor system. The default setting is the configuration from EPCQ device using the Active Serial Standard Configuration Scheme. (ON = ‘0’ / OFF = ‘1’)

MSEL	P18	AS-Standard
0	1	OFF
1	2	OFF
2	3	ON
3	4	ON
4	5	OFF

Table 2

Clocking

The clock scheme of the "SoCrates Evaluation Board" is build around an IDT EEPROM programmable clock generator 5V49EE904. This device has two clock sources and 9 programmable outputs. One clock input is connected to a 25MHz crystal, and the second input is connected to a MMCX connector (P15) to be feed with an external clock source. The device is already programmed according to the requirements of the board. Table 3 shows the outputs of the clock driver.

The connector P17 (Table 4) provides the I²C Interface to the 5V49EE904 device. Using the IDT evaluation board's I²C interface the device can be easily reprogrammed.

Clock Driver Outputs

IO-pin	Clock	Voltage
30 / Out0	CLK25 - Phy	3.3V
7 / Out1	CLK50 - FPGA	3.3V
8 / Out2	CLK24 - USB-Blaster	3.3V
24 / Out3	CLK26 - USB PHY	3.3V
10 / Out4	CLK12 - USB/UART	1.8V
14 / Out5	CLK25 - HPS	2.5V
23 / Out6	CLK50 - FPGA	3.3V

Table 3

FPGA Clock Sources

Function	FPGA Pin	FPGA Signal
50MHz	Y13	
50MHz	Y15	
50MHz	V11	
50MHz	V12	
25Mhz	E20	HPS-Clock1
25Mhz	D20	HPS-Clock2

Table 4

IDT Clock Buffer I²C Interface (P17)

Pin	Function
1	GND
2	SDA
3	SCLK

Table 5

Power Supply

The SoCrates Evaluation Board allows to supply the board from an unregulated power supply (7.5V ... 36V). The plug connected to P11 must be of type "center positive". A LMZ14203 switching module is used to generate a 5V power rail, which is used to feed the regulators for the lower voltages. Four LMZ2 modules are used to generate the voltages: 3.3V, 1.35V, and 1.1V for the FPGA and the HPS. Linear Regulators are used to generate the 1.8V for the USB Phy and 2.5V for the FPGA analog parts. A TPS51200 is used to generate the DDR reference voltage and the DDR termination voltage.
Power sequencing is implemented to power up the Core Voltages (1.1V) first, then the I/O Voltages.

A "Power Good" signal is generated to signal that all voltages are in the valid ranges.

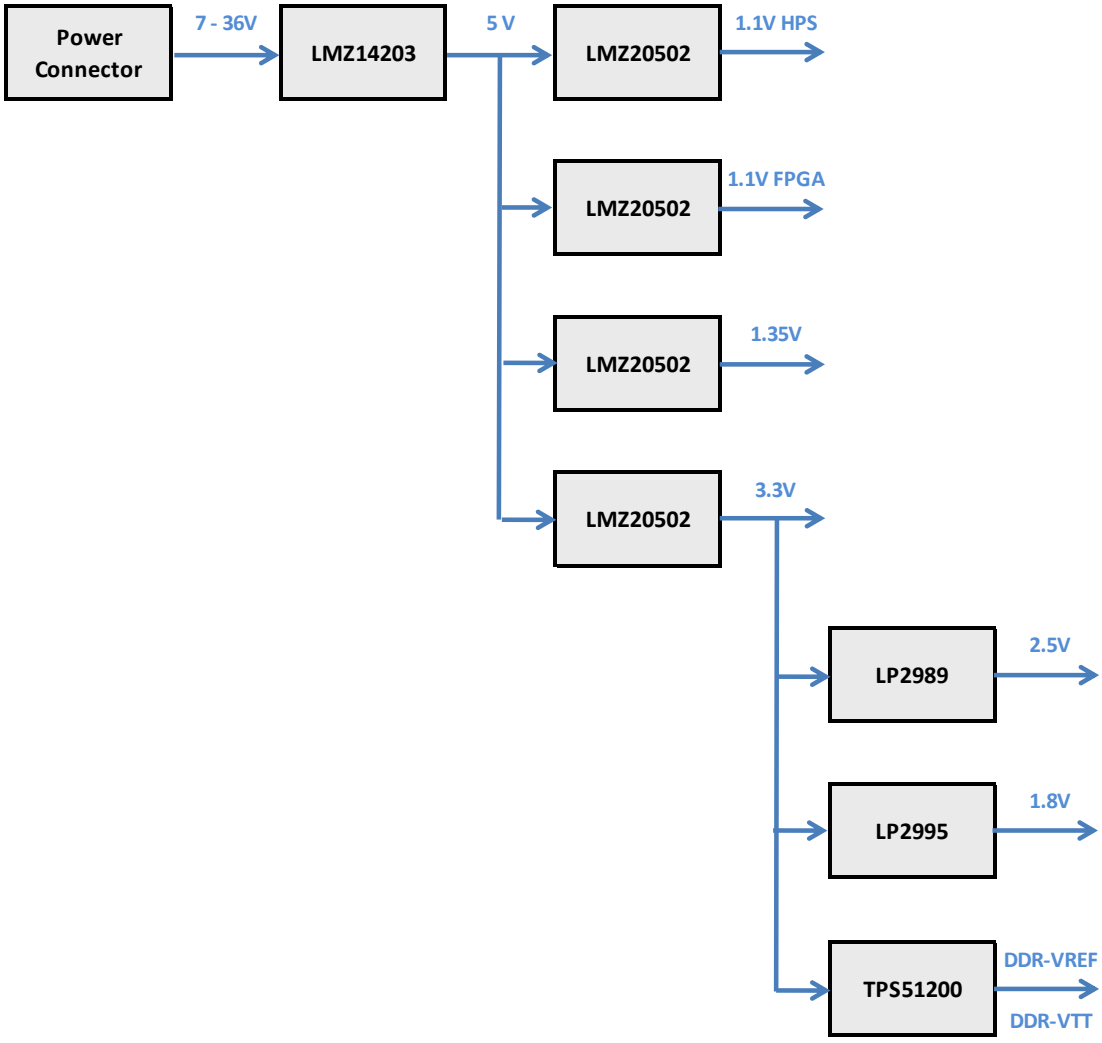


Figure 4

Reset Signal

Function	Pin	Signal Name
Power Good	H19	HPS-NPOR
Power Good	AB25	RSTn

Table 6

VBAT

The power supply for the battery backup of the FPGA can be connected to Pin-Header P4. The VBAT pin must be connected to supply voltage to start the FPGA. If no external battery backup is required insert a jumper between Pin 1 and Pin 2. This connects the 2.5V rail to the VBAT signal. If you would like to power VBAT with an external voltage use Pin 2 for the supply voltage and Pin 3 as a GND reference pin.

If VBAT is not connected to any voltage, the FPGA will not be accessible!!!

Pin	Function
1	2.5V Board supply
2	VBAT
3	GND

Table 7

HPS Subsystem

The figure below shows the HPS Peripheral Pin multiplexing for the SoCrates Board.

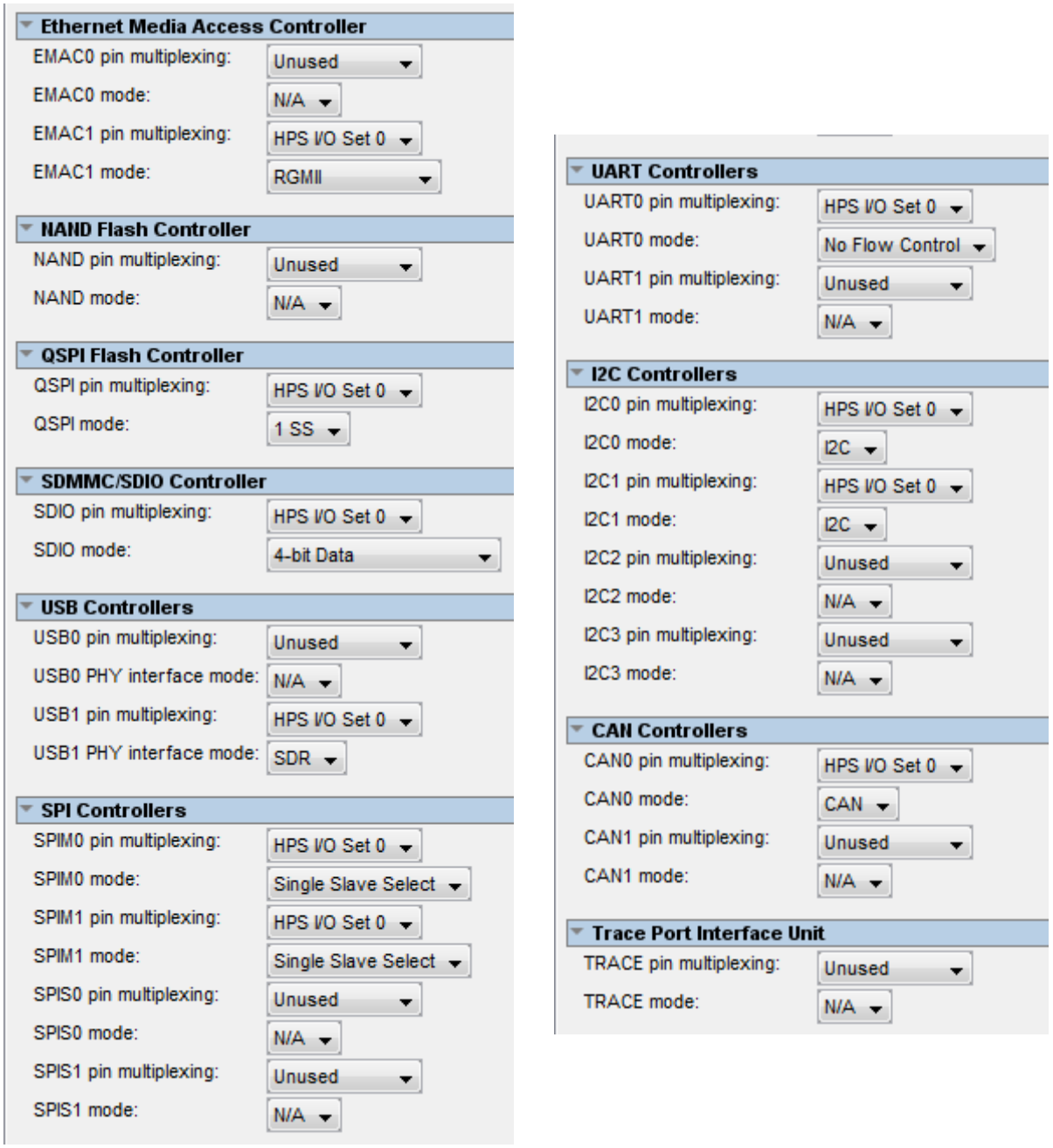


Figure 5

DDR3 Memory

SoCrates is equipped with 1Gbyte DDR3 memory. The Micron MT41K256M32SLD-125 device is used. The memory interface is clocked at 333.33MHz using the 1.35V DDR3L standard. Figure 6 shows the memory settings in Qsys. A Preset is available for all the memory settings for the SoCrates board.

This device is obsolete and should not be used for new developments.

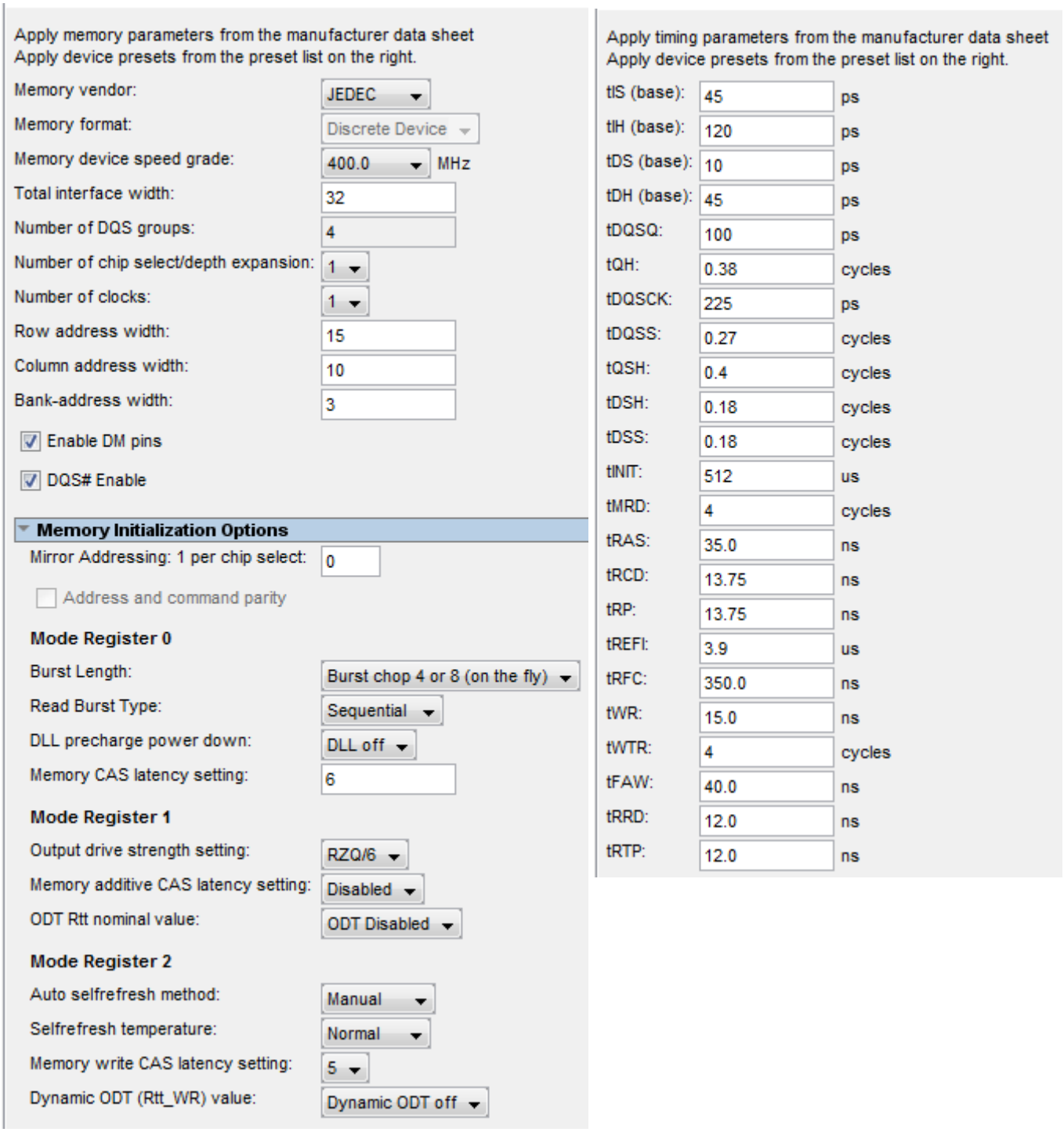


Figure 6

SDCard Interface

The SDCard interface is connected to the HPS System and uses the interface in a 4 bit mode. The “Write Protect” switch is connected to GPIO00.

SDCard (P8) FPGA Connection

Function	Pin	FPGA Pin
HPS-SDIO-CLK		B8
HPS-SDIO-CMD		D14
HPS-SDIO-D0		C13
HPS-SDIO-D1		B6
HPS-SDIO-D2		B11
HPS-SDIO-D3		B9
Protect Switch	GPIO00	E4

Table 8

QSPI Flash

An EPCQ256 Flash device can be used for booting the HPS. The QSPI Flash is connected to the QSPI Port of the HPS.

QSPI (U27) FPGA Connection

Function	Pin	FPGA Pin
HPS-QSPI-CS		A6
HPS-QSPI-CLK		C14
HPS-QSPI-D0		A8
HPS-QSPI-D1		H16
HPS-QSPI-D2		A7
HPS-QSPI-D3		J16

Table 9

USB Phy

A Texas Instruments TUSB1210 USB Phy is used on the SoCrates Evaluation Board. This Phy is connected to the SoC device using an eight bit parallel interface with 1.8V IO standard.

USB Phy (U16) FPGA Connection

Function	Pin	FPGA Pin
USB-D0		C10
USB-D1		F5
USB-D2		C9
USB-D3		C4
USB-D4		C8
USB-D5		D4
USB-D6		C7
USB-D7		F4
USB-CLK		G4
USB-NXT		D5
USB-DIR		E5

USB-STP		C5

Table 10

Ethernet Phy

For the "Ethernet Connectivity" a Lantiq PEF7071 Gigabit Ethernet Phy is used. The RJ45 connector P9 has an integrated transformer. Two LEDs to show the status are available within the RJ45 connector, and a third LED is available on the board (D5)

Ethernet Phy (U14) FPGA Connection

Function	Pin	FPGA Pin
MDC		E16
MDIO		A13
TX_CLK		J15
TXD0		A16
TXD1		J14
TXD2		A15
TXD3		D17
TX_CTL		Â12
RX_CLK		J12
RX_CTL		J13
RXD0		A14
RXD1		A11
RXD2		C15
RXD3		A9
Interrupt	GPIO35	B14

Table 11

UART

The UART of the HPS is available on the one hand on connector P14 (Pin-Header) and on the other hand uses an interface device to directly translate to USB standard which allows direct connection to a PC over connector P7.

Function	Pin	FPGA Pin
HPS_UART_RX		A22
HPS_UART_TX		B21

UART on P14

These signals are coming directly from the SoC device and no Phy is used. To provide a standard RS232 interface, a level shifter must be added externally (!). Table 12 shows a part of the pin assignment of connector P14

Function	Pin	Pin	Function
HPS_SDIO_D4	29	30	HPS_USB_TX
HPS_SDIO_D6	31	30	HPS_USB_RX

Table 12

UART to USB Converter

A Texas Instruments TUSB3410 USB Converter is used to convert the serial to USB protocol. The USB protocol is available on a standard USB Header for direct connection to a PC. The TUSB3410 is powered via USB. The UART Signals are available on the mini USB connector P7.

CAN Phy

A TJA1043 CAN driver from NXP is used for the HPS-CAN core. A 60 Ohm termination resistor is available on the board. A respective cabling can be used to integrate the termination resistor. Table 12 shows controlling signals of the FPGA and Table 14 an extract of the pin assignment at connector P14.

CAN Phy (U22) FPGA Connection

Function	Pin	FPGA Pin
HPS-CAN-RX		A17
HPS-CAN-TX		H17
CAN-Wake	GPIO53	A20
CAN_CSCK	SPI_CLK	C19
CAN_CSDI	SPI_MISO	B19
CAN_CSDO	SPI_MOSI	B16
CAN_C1CS	SPI_CC0	C16

Table 13

CAN Connector (P14)

Function	Pin	Pin	Function
CAN-BAT	1	2	VCC5
RES 60R	3	4	RES 60R
CANH	5	6	CANL
GND	7	8	GND

Table 14

DIP Switch

The SoCrates Evaluation Board is equipped with a DIP switch with 8 switches. Every switch has a pull-down resistor and switch to high level in “ON” state. The Dip Switch is connected to the "General Purpose Inputs" (GPI) of the HPS System.

Dip-Switch (P3) FPGA Connection

Function	Pin	FPGA Pin
Switch 1	GPI0	M25
Switch 2	GPI4	R28
Switch 3	GPI8	Y28
Switch 4	GPI13	V24
Switch 5	GPI5	P26
Switch 6	GPI3	R21
Switch 7	GPI9	Y26

Switch 8	GPI12	AC27

Table 15

Navigation Key

The SoCrates Evaluation Board is equipped with a 5 button navigation key. The switch has pull-down resistors and switch to high Level in “ON” State.

Navigation Key (P20) FPGA Connection

Function	Pin	FPGA Pin
Switch Up	GPI6	T17
Switch Down	GPI7	T16
Switch Left	GPI11	U16
Switch Right	GPI10	U15
Switch Button	GPI2	R20

Table 16

User LEDs

On the board 3 USER LEDs are available. A logic zero will light the LED.

User LEDs

Function	Pin	FPGA Pin
LED 0	GPIO28	D15
LED 1	GPIO48	C21
LED 2	GPIO54	J18

Table 17

RTC

A M41T82M RTC circuit from STM is implemented on the SoCrates Evaluation Board which uses an I²C interface. The RTC is connected to a GoldCap (33mF) for backup voltage. This will keep the RTC running for about 60 days – without any power supply.

RTC (U15) FPGA Connection

Function	Pin	FPGA Pin
RSTn	GPI1	K27
HPS-I²C0_SCL		C18
HPS-I²C0_SDA		A19

Table 18

GPIO

All spare IO pins of the HPS are connected to Pin-Header P14. The complete pin assignement of P14 is shown in table 19. This connector is a 2.54mm Pin-Header on the bottom side of the board.

GPIO P14 FPGA connection

Function	Pin	Pin	Function
CAN-BAT	1	2	VCC5
RES 60R	3	4	RES 60R
CANH	5	6	CANL
GND	7	8	GND
	9	10	HPS_GPIO28
HPS_GPIO48	11	12	HPS_GPIO54
HPS-I²C1_SCL	13	14	HPS-I²C1_SDA
HPS-SPIM0_MISO	15	16	HPS-SPIM0_SS0
HPS-SPIM0_MOSI	17	18	HPS-SPIM0_CLK
HPS_SDIO_PWR	19	20	
GND	21	22	GND
HPS_GPIO9	23	24	HPS-GPIO44
HPS_SDIO_D5	25	26	
HPS_SDIO_D7	27	28	GND
HPS_SDIO_D4	29	30	HPS_UART_TX
HPS_SDIO_D6	21	32	HPS_UART_RX

Table 19

FPGA Connections

IOBANK3B

The signals of IOBANK3 are connected to Pin-Header P12. This connector is a 2.54mm Pin-Header on the bottom side of the board. The IOBANK is supplied with 3.3V.

Function	FPGA	Pin	Pin	FPGA	Function
		1	2		
GND		3	4		VCC33
IOB3B0	AE12	5	6	AD12	IOB3B1
IOB3B2	AE11	7	8	AD11	IOB3B3
IOB3B4	AD10	9	10	AF11	IOB3B5
IOB3B6	AF9	11	12	AF10	IOB3B7
IOB3B8	AE9	13	14	AF8	IOB3B9
IOB3B10	AE7	15	16	AE8	IOB3B11
IOB3B12	AF6	17	18	W12	IOB3B13
IOB3B14	W11	19	20	AF5	IOB3B15
GND		21	22		VCC33
GND		23	24		VCC33
IOB3B16	T12	25	26	T13	IOB3B17
IOB3B18	U11	27	28	T11	IOB3B19
IOB3B20	AF7	29	30	AH6	IOB3B21
IOB3B22	AG6	31	32	AH5	IOB3B23
IOB3B24	AG5	33	34	AH4	IOB3B25
IOB3B26	AF4	35	36	AH3	IOB3B27
IOB3B28	AH2	37	38	AE4	IOB3B29
GND		39	40		VCC33

Table 20

IOBANK4A

The signals of IOBANK4 are connected to Pin-Header P13. P13 is a 1.27mm Pin-Header on the top side of the board. Four Signals of this IOBANK are used for the ΣΔ-ADC/DAC subsystem. This IOBANK is supplied with 3.3V but can also be supplied externally by changing the resistors R72 and R73. Eight I/O Pins are connected to LEDs in parallel.

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		VCC33
IOB4A0	AH7	3	4	AG8	IOB4A1
IOB4A2	AH8	5	6	AG9	IOB4A3
IOB4A4	AH9	7	8	AG10	IOB4A5
IOB4A6	AG11	9	10	AH11	IOB4A7
GND		11	12		VCC33
IOB4A8	AF13	13	14	AH12	IOB4A9
IOB4A10	AG13	15	16	AH13	IOB4A11
IOB4A12	AG14	17	18	AH14	IOB4A13
IOB4A14	AG15	19	20	AG16	IOB4A15
GND		21	22		VCC33
IOB4A16	AH16	23	24	AF17	IOB4A17
IOB4A18	AH17	25	26	AG18	IOB4A19
IOB4A20	AH18	27	28	AG19	IOB4A21
IOB4A22	AH19	29	30	AG20	IOB4A23
GND		31	32		VCC33
IOB4A24	AG21	33	34	AF20	IOB4A25
IOB4A26	AE20	35	36	AF21	IOB4A27
IOB4A28	AE22	37	38	AE23	IOB4A29
IOB4A30	AF23	39	40	AE24	IOB4A31

Table 21

USER LEDs

Eight USER LEDs are connected to Signals of IOBANK4A. These signals are connected to P13 in parallel.

USER LED FPGA Connection

Function	Pin	FPGA Pin	Pin at P13
LED0	IOB4A0	AH7	3
LED1	IOB4A4	AH9	7
LED2	IOB4A8	AF13	13
LED3	IOB4A12	AG14	17
LED4	IOB4A16	AH16	23
LED5	IOB4A20	AH18	27
LED6	IOB4A24	AG21	33
LED7	IOB4A28	AE22	37

Table 22

ΣΔ-ADC / DAC Subsystem

Missing Link Electronics provides an IP-Core for ΣΔ-ADC / DAC technology using LVDS Input Signals and 3.3V IO. SoCrates implements two ADC channels and two DAC channels. The DAC subsystem uses two IO Signals from IOBANK4A with a RC Low pass filter. The ADC requires two LVDS Inputs and two REF outputs from IOBANK4A.To get a higher resolution it is possible to provide an external VCCIO voltage for IOBANK4A.

FPGA Connection (IOBANK4A)

Function	Pin	FPGA Pin
SD_Out0		U13
SD_Out1		U14
SD_REF0		V13
SD_REF1		W14

Table 23

FPGA Connection (IOBANK8A)

Function		FPGA Pin
LVDS_IN_SD0N		D11
LVDS_IN_SD0P	1.65V	E11
LVDS_IN_SD1N		C12
LVDS_IN_SD1P	1.65V	D12

Table 24

ΣΔ-ADC / DAC Connector (P1)

Function	Pin	Pin	Function
VCCIO	1	2	GND
AIN1	3	4	AOUT1
GND	5	6	GND
AIN2	7	8	AOUT2
GND	9	10	GND

Table 25

EBV Observer Connector

The EBV Observer CMOS Sensor Development Platform provides several CMOS Sensor boards with a standardized Pin-Header. These modules can be used on SoCrates too. The Pin-Header (P10) provides several LVDS Channels and additional 3.3V GPIO Signals. SoCrates is assembled with a Samtec QSH-030-01-L-A-K connector.

CMOS Sensor Pin-Header (P10)

Function	FPGA	Pin	Pin	FPGA	Function
VCC5		1	2		GND
VCC5		3	4		GND
VCC5		5	6		GND
VCC5		7	8		GND
GND		9	10		GND
IO0	AD20	11	12	AA19	IO1
IO2	AA18	13	14	AD19	IO3
IO4	AE19	15	16	AF18	IO5
GND		17	18		GND
ID0	AD4	19	20	Y24	LVDS_CLK_INP
ID1	AC4	21	22	W24	LVDS_CLKINN
GND		23	24		GND
LVDS_IN2P	Y17	25	26	AA20	LVDS_IN0P
LVDS_IN2N	Y18	27	28	W20	LVDS_IN0N
LVDS_IN3P	Y16	29	30	AA20	LVDS_IN1P
LVDS_IN3N	W15	31	32	Y19	LVDS_IN1N
GND		33	34		GND
		35	36		
		37	38		
LVDS_IN4P	Y11	39	40	V16	LVDS_IN6P
LVDS_IN4N	AA11	41	42	V15	LVDS_IN6N
GND		43	44		GND
LVDS_IN5P	U10	45	46	W8	LVDS_IN7P
LVDS_IN5N	V10	47	48	Y8	LVDS_IN7N
LVDS_CLK_OUTP	AB26	49	50	U9	LVDS_IN8P
LVDS_CLK_OUTN	AA26	51	52	T8	LVDS_IN8N
GND		53	54		GND
IO6	AE15	55	56	AE17	IO7
IO8	AA15	57	58	AD17	IO9
IO10	AA13	59	60	AF15	IO11

Table 26

FPGA Connection Temperature Sensor

The measurement of temperature is accomplished with a sensor from National Semiconductor LM74. This device has a SPI / Microwire compatible interface. The LM74 has a resolution of 12 bits.

FPGA Connection

Function	Device	FPGA Pin
TS/O		D8
TSCL		E8
TCSn		Y4

Table 27

LVDS TFT Interface

SoCrates provided a Pin-Header to connect LVDS based TFT Displays directly. The interface provides one differential clock signal and 3 differential data signals. Additionally four 3.3V GPIO signals are available for touch controller interface or dimming of the backlight. The connector type is a DF19G-30P and the pin assignment is shown in Table 28.

FPGA Connection (P2)

Function	Pin	FPGA Pin
VCC33	1	
VCC33	2	
GND	3	
GND	4	
LVDS_TFT0N	5	AB23
LVDS_TFT0P	6	AC24
GND	7	
LVDS_TFT1N	8	AE26
LVDS_TFT1P	9	AF26
GND	10	
LVDS_TFT2N	11	AD26
LVDS_TFT2P	12	AE25
GND	13	
LVDS_CLKN	14	AA23
LVDS_CLKP	15	AA24
GND	16	
	17	
	18	
GND	19	
GND	20	
VCC33	21	
TC3	22	AE6
TC2	23	AD5
TC1	24	AB4
TC0	25	AA4
GND	26	
VCC5	27	
VCC5	28	
GND	29	
GND	30	

Table 28

Bill of Material

Description	Manufacturer	Part Number	Count	Reference Designator
CY7C68013A-56LTXC	Cypress Semiconductor	CY7C68013A-56LTXC	1	U7
5V49EE904NLGI	IDT (Integrated Device Technology)	5V49EE904NLGI	1	U8
M41T82ZM6E	STMicroelectronics	M41T82ZM6E	1	U15
PEF7071V V1.5/LAN	Lantiq	PEF7071V V1.5	1	U19
EPCQ256SI16N	Altera Corporation	EPCQ256SI16N	2	U3 U27
EPM570F100C5N	Altera Corporation	EPM570F100C5N	1	U13
5CSXFC6C6U23C8NES	Altera Corporation	5CSXFC6C6U23C8NES	1	U1
SN65220DBVT	Texas Instruments	SN65220DBVT	3	U6 U11 U14
SN74AVCH1T45DCKT	Texas Instruments	SN74AVCH1T45DCKT	1	U29
REF3033AIDBZTG4	Texas Instruments	REF3033AIDBZTG4	1	U21
LMZ20501	Texas Instruments	LMZ20501SYE/NOPB	1	U10
TPS51200DRCT	Texas Instruments	TPS51200DRCT	1	U9
LMR62014XMFE/NOPB	Texas Instruments	LMR62014XMFE/NOPB	1	U28
LMZ20502	Texas Instruments	LMZ20502SYE/NOPB	3	U4 U5 U18
TPS2553DBV	Texas Instruments	TPS2553DBV	1	U24
TUSB1210BRHBT	Texas Instruments	TUSB1210BRHBT	1	U16
TUSB3410VF	Texas Instruments	TUSB3410VF	1	U12
TPS76933DBVT	Texas Instruments	TPS76933DBVT	1	U26
LM74	Texas Instruments	LM74CIM-3/NOPB	1	U20
LP2989IM-2.5	Texas Instruments	LP2989IM-2.5/NOPB	1	U31
LP2992AIM5-1.8	Texas Instruments	LP2992AIM5-1.8	1	U23
LMZ14203TZE-ADJ	Texas Instruments	LMZ14203TZE-ADJ	1	U32
MT41K256M32SLD-125:E	Micron Technology Inc.	MT41K256M32SLD-125:E	1	U2
TJA1145	NXP Semiconductors	TJA1145	1	U22
D_STPS2H100A	STMicroelectronics	STPS2H100A	1	D6
LED 0603_Blau	Avago Technologies	HSMR-CL25	5	D5 D16 D42 D44 D45
LED 0603_GREEN 5mA			15	D1 D3 D7 D8 D14 D15 D17 D18 D19 D20 D21 D22 D23 D24 D25
BAT54SWT1G	ON Semiconductor	BAT54SWT1G	5	D10 D11 D12 D13 D27
BAT54H,115 (SOD123)	NXP Semiconductors	BAT54H,115	1	D2
D-CRS08	TOSHIBA	CRS08	1	D26
BC850B	NXP Semiconductors	BC850B	2	U39 U40
Crystal QUARZ 1.9 X 5MM SMD CER 32.768KHZ 9.0	Micro Crystal	CC4V-T1A 32.768KHZ +-20PPM 9PF	1	U17
OSC25.00 MHz	Fox Electronics	FQ3225B-25	1	U25
R0603_1K00A1%0			10	R18 R19 R20 R21 R35 R36 R43 R74 R89 R110

Description	Manufacturer	Part Number	Count	Reference Designator
R0603_1K50A1%0			1	R78
R0603_2K00A1%0			2	R12 R14
R0603_2K20A1%0			1	R106
R0603_4K87A1%0			3	R162 R171 R173
R0603_10K0A1%0			40	R1 R2 R3 R4 R5 R9 R13 R46 R47 R52 R54 R56 R57 R59 R60 R61 R68 R69 R71 R77 R79 R80 R82 R83 R86 R92 R93 R94 R95 R100 R111 R121 R122 R123 R124 R125 R126 R127 R153 R154
R0603_12K0A1%0			2	R107 R151
R0603_20K0A1%0			1	R11
R0603_60R4A1%0			1	R34
R0603_100KA1%0			2	R104 R168
R0603_330RA1%0			16	R30 R31 R32 R37 R38 R49 R50 R66 R75 R76 R96 R98 R99 R101 R102 R103
R0603_470RA1%0			4	R155 R156 R164 R165
R0603_4K70A1%0			5	R15 R16 R29 R141 R142
R0603_5K60A1%0			1	R134
R0603_24K0A1%0			1	R105
R0603_15KA1%0			1	R81
R0603_33R0A1%0			2	R84 R85
R0603_47K0A1%0			2	R137 R169
R0603_11K0A1%0			3	R62 R64 R70
R0603_49K9			2	R39 R51
R0603_120KA1%0			1	R133
R0603_270KA1%0			4	R40 R41 R45 R58
R0603_8K66A1%			1	R65
R0603_16K0A1%0			2	R90 R91
R0603_5R10A1%0			1	R63
R0603_180KA1%0			2	R130 R166
R0603_62K0A1%0			1	R150
R0603_210K0A1%0			1	R136
R0603_150KA1%0			3	R131 R132 R167
R0603_1K07A1%0			1	R135
R0603_240RA1%0			4	R24 R25 R87 R88
R0603_39R0A1%0			8	R139 R140 R145 R146 R147 R149 R157 R158
R0603_56K2A1%0			1	R152
R0805_1M00A1%0			3	R8 R44 R53
R0805_0R00A1%0			1	R72
R0402_0R00A1%0			8	R7 R17 R23 R27 R28 R109 R179 R181
R0402_100RA1%0			2	R42 R180

Description	Manufacturer	Part Number	Count	Reference Designator
R0402_51R0A1%0			5	R113 R114 R115 R116 R117
R0402_240R0A1%0			3	R48 R55 R163
RN0402x8_51R			3	RN3 RN5 RN6
C0603_10N0A50V			10	C6 C66 C70 C118 C120 C174 C190 C191 C192 C225
C0603_100PA50V			2	C20 C33
C0603_33N0A50V			2	C18 C19
C0603_18P0A50V			4	C26 C28 C52
C0603_33P0A50V			1	C2
C0603_330PA50V			2	C12 C73
C0603_22N0A50V			2	C54 C72
C0603_10U0A6V3			57	C24 C29 C31 C34 C35 C36 C37 C39 C41 C42 C43 C46 C47 C48 C49 C50 C53 C56 C63 C64 C65 C67 C68 C74 C75 C76 C77 C78 C79 C80 C81 C86 C87 C88 C96 C98 C102 C103 C104 C105 C106 C107 C154 C155 C156 C157 C158 C159 C171 C172 C175 C178 C198 C205 C220 C221 C222
C0603_1N00A100V			1	C21
C0603_2U20A10V			6	C1 C3 C57 C195 C196 C197
C0603_27P0A50V			1	C30
C0603_270PA50V			1	C40
C0805_22U0A6V3			4	C23 C25 C27 C51
C0805_10U0A10V			2	C71 C38
C1206_1N00A2KV			3	C11 C13 C15
C7343_33U0A35VP			2	C32 C240
C1210_22U_16V			4	C55 C59 C83 C144
CTZV-_333UA35VP			1	C109
C1210_4U70A50V			2	C113 C121

Description	Manufacturer	Part Number	Count	Reference Designator
C0402_100NA25V			93	C4 C5 C7 C8 C9 C10 C14 C16 C22 C44 C45 C60 C61 C62 C69 C82 C84 C85 C89 C90 C91 C92 C93 C94 C95 C97 C99 C100 C101 C108 C110 C111 C112 C117 C119 C125 C126 C127 C130 C131 C133 C134 C135 C145 C146 C147 D148 C149 C150 C151 C153 C160 C161 D162 C163 C164 C165 C166 C167 C168 C169 C170 C173 C176 C183 C184 C185 C186 C187 C188 C189 C193 C194 C199 C200 C201 C202 C203 C204 C206 C207 C208 C209 C210 C211 C212 C214 C215 C217 C218 C219 C223 C224
CTZV-_33MA2V6			1	C17
L0603_10NHA0A4	EPCOS	B82496C3100J	4	L2 L3 L4 L6
L1206_4U70AA34	MURATA	LQH31MN4R7K03L	1	L5
744222	Würth Elektronik eiSos GmbH & Co. KG	744222	1	L11
LWE-T_10U0A1A4	Würth Elektronik eiSos GmbH & Co. KG	744062100	1	L1
USB_MINI_AB	Molex	56579-0576	3	P5 P6 P7
TSM-105-01-L-DV-ATSM-105-01-L-DV-A	Samtec	TSM-105-01-L-DV-A	1	P1
TSM-120-01-L-DV-A	Samtec	TSM-120-01-L-DV-A	1	P12
TSM-116-01-L-DV-A	Samtec	TSM-116-01-L-DV-A	1	P14
Micro SDCard Socket			1	P8
MMCX-J-P-H-ST-SM1	Samtec	MMCX-J-P-H-ST-SM1-K	1	P15
TFM-120-02-S-D-LC-P	Samtec	TFM-120-02-S-D-LC-P	1	P13
DF19G-30P-1H	HRS (Hirose)	DF19G-30P-1H(54)	1	P2
QSH-030-01-L-D-A-K	Samtec	QSH-030-01-L-D-A-K	1	P10
DC10A	Cliff Electronic Components	DC10A	1	P11
Pin Header 3 Pin			3	P4 P17 P18
7499111614A	Würth Elektronik eiSos GmbH & Co. KG	7499111614A	1	P9
TPA511G	C&K Components	TPA511G	1	P20
FSM2JSMA	TE Connectivity	FSM2JSMA	1	P24
SW-08-SMD	TE Connectivity	4-1825059-2	1	P3
Testpoint SMD	Keystone Electronics	5015	1	P16

Schematics

If you need better quality of the schematic, please download the schematic and silk information in PCAD-2006 format from www.devboards.de/download

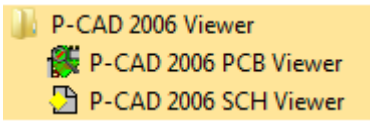
A respective viewer application can be downloaded from:

http://www.altium.com/community/downloads/legacy_p-cad.cfm

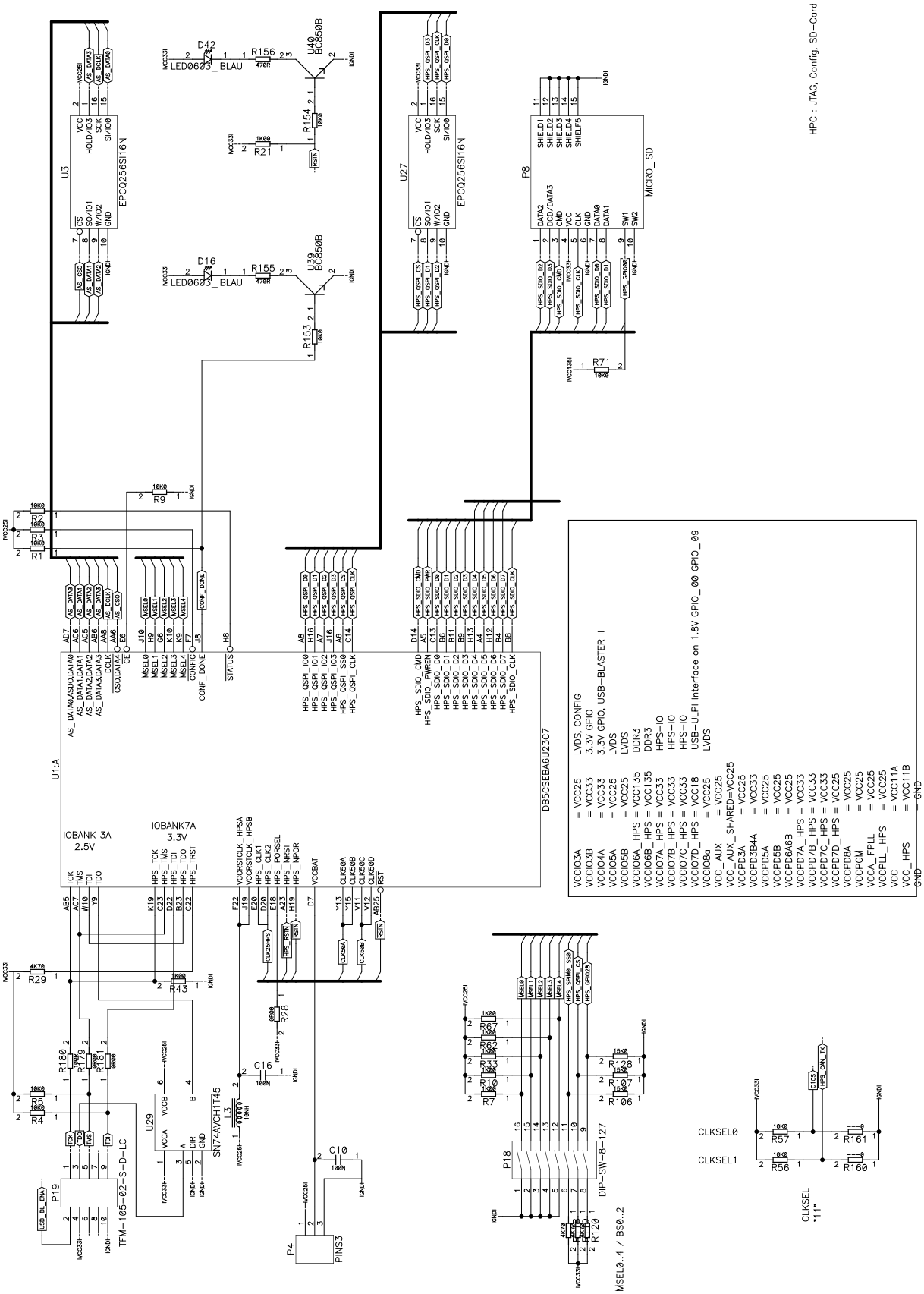
P-CAD Viewer

P-CAD 2006 Viewer (9,908 KB)
The P-CAD 2006 freeware* Viewer works with P-CAD 2006 (including Service Pack 1 and 2), P-CAD 2004, P-CAD 2002, P-CAD 2001 and P-CAD 2000 schematic & PCB files, as well as ACCEL EDA V15 schematic & PCB files.

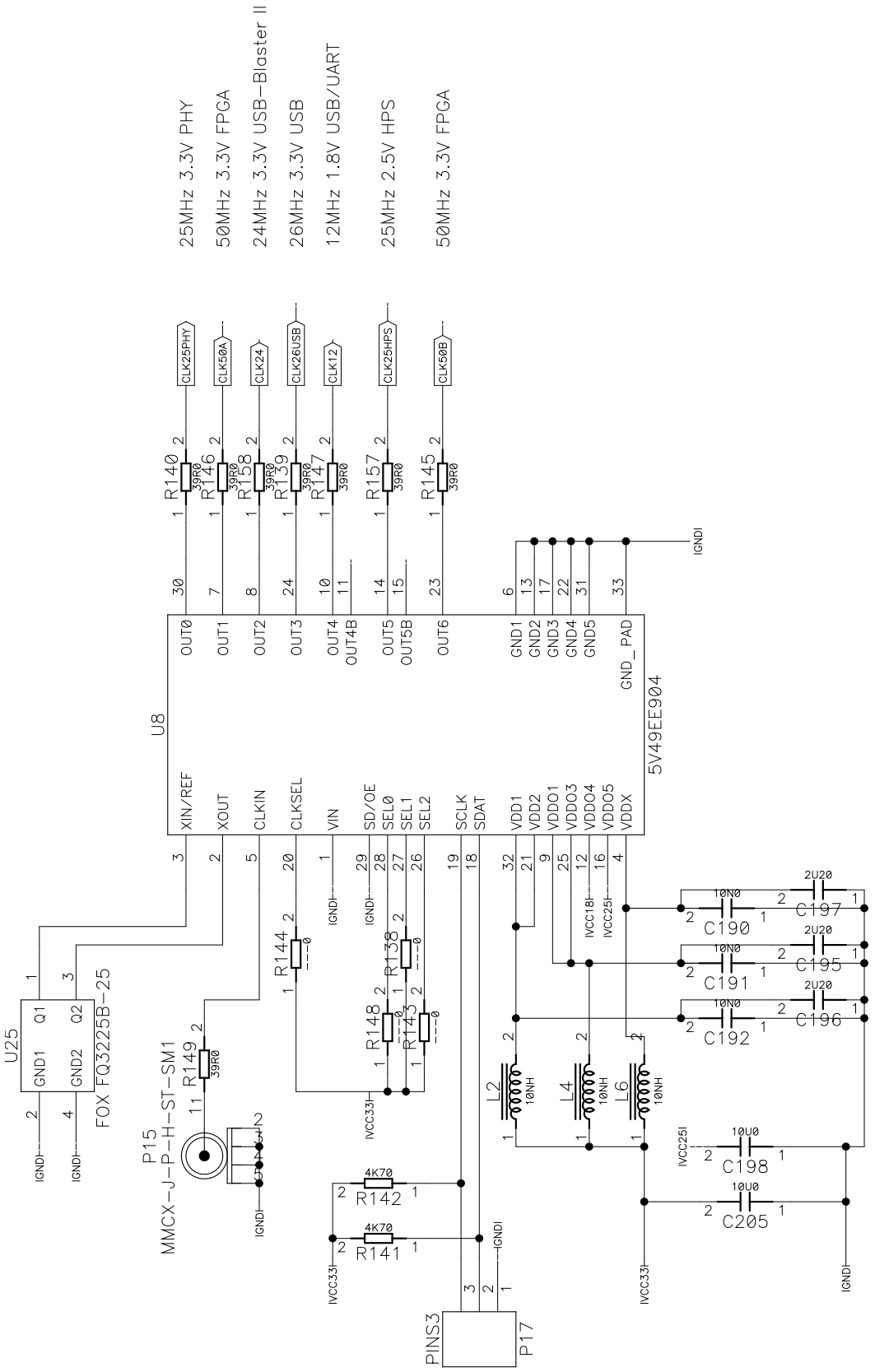
After installing you can find the schematic and layout viewer in your Start Menu:



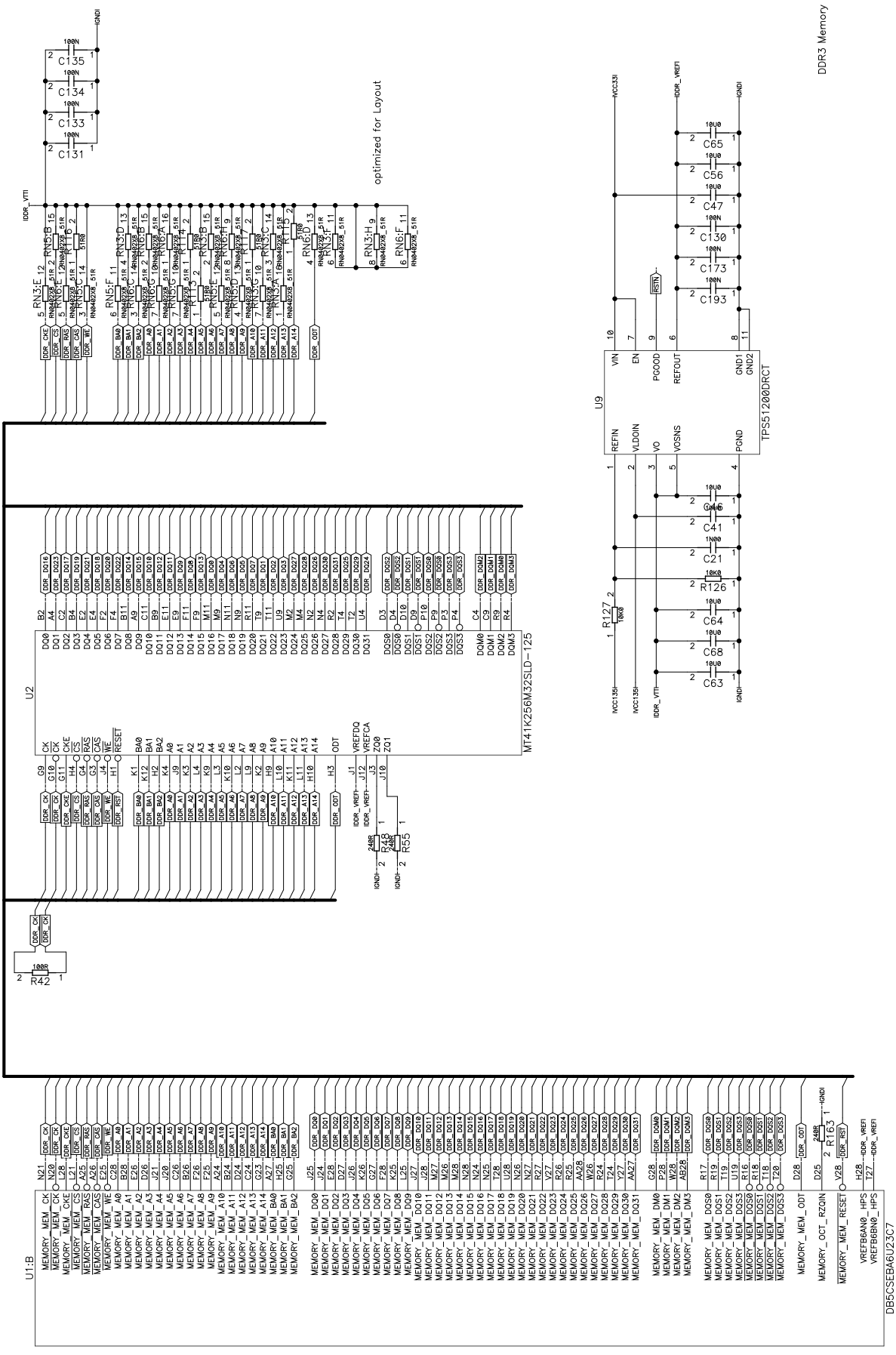
HPS, JTAG, Config, SDCard



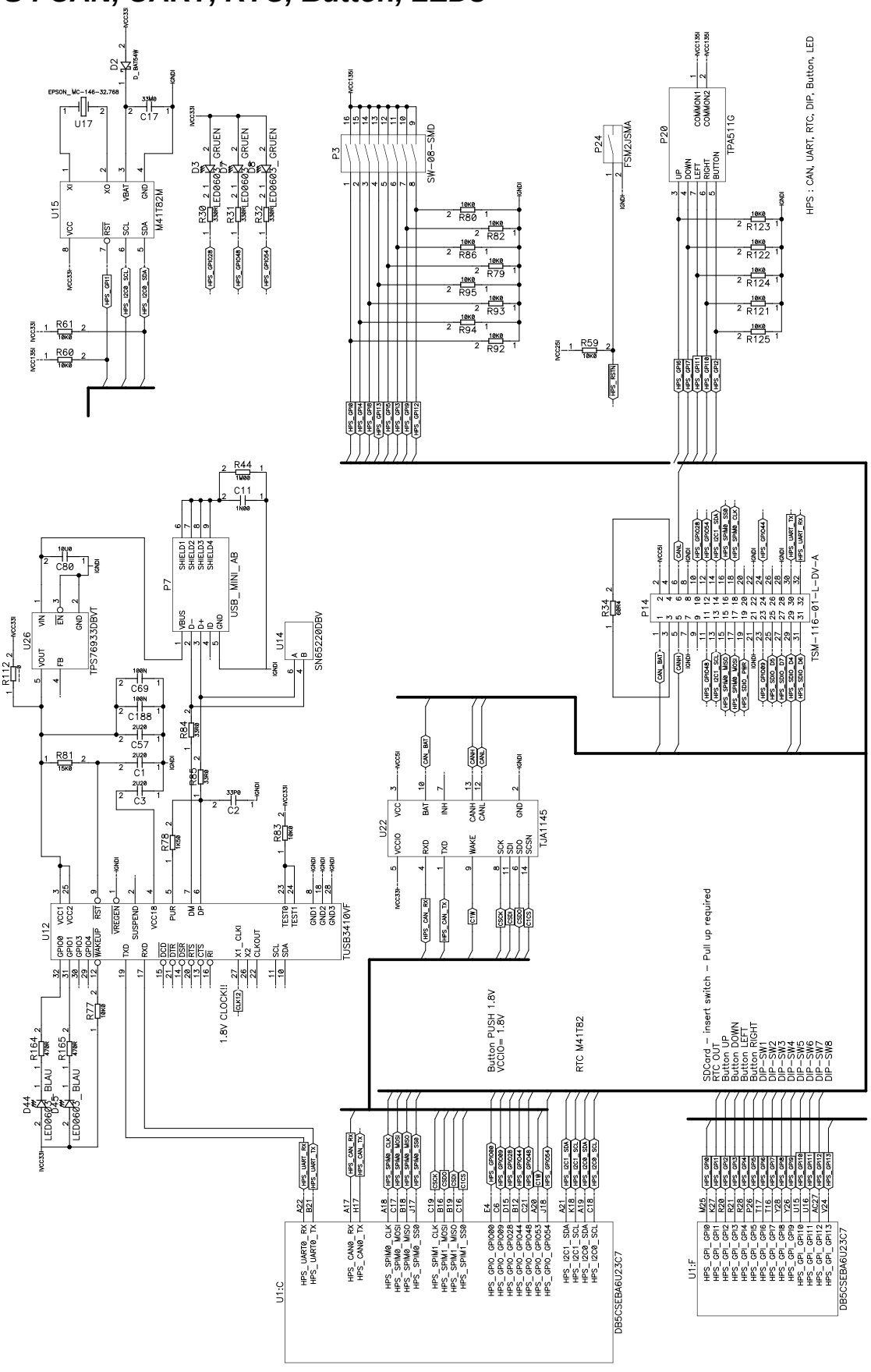
Clocking


25MHz 3.3V PHY
50MHz 3.3V FPGA
24MHz 3.3V USB-Blaster II
26MHz 3.3V USB
12MHz 1.8V USB/UART
25MHz 2.5V HPS
50MHz 3.3V FPGA
U8
5V49EE904
U25
FOX FQ3225B-25
P15
MMCX-J-P-H-ST-SM1
P17
PINS3
IGND
IVCC33
IVCC25
IVCC18

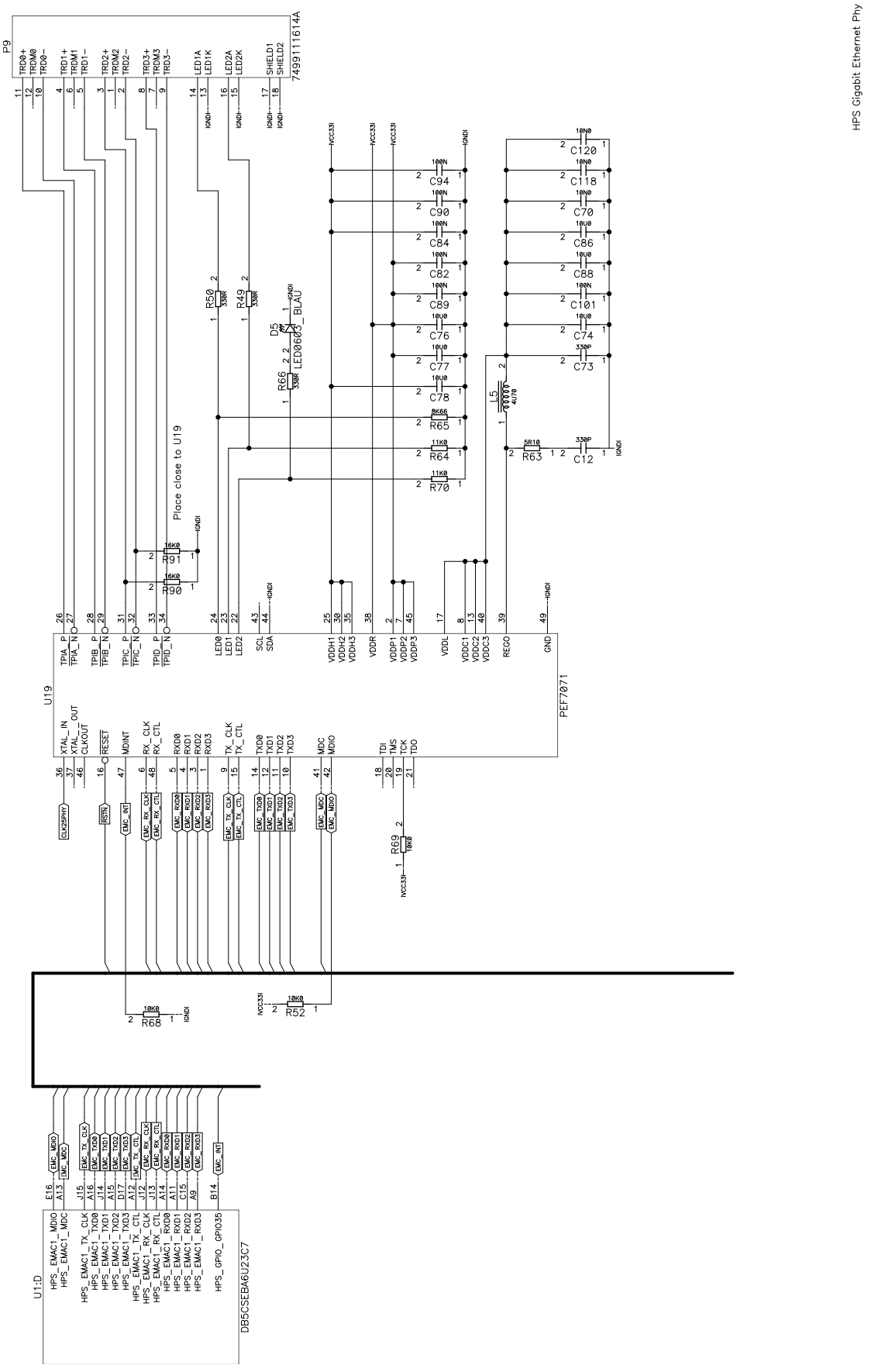
HPS : DDR3 Memory



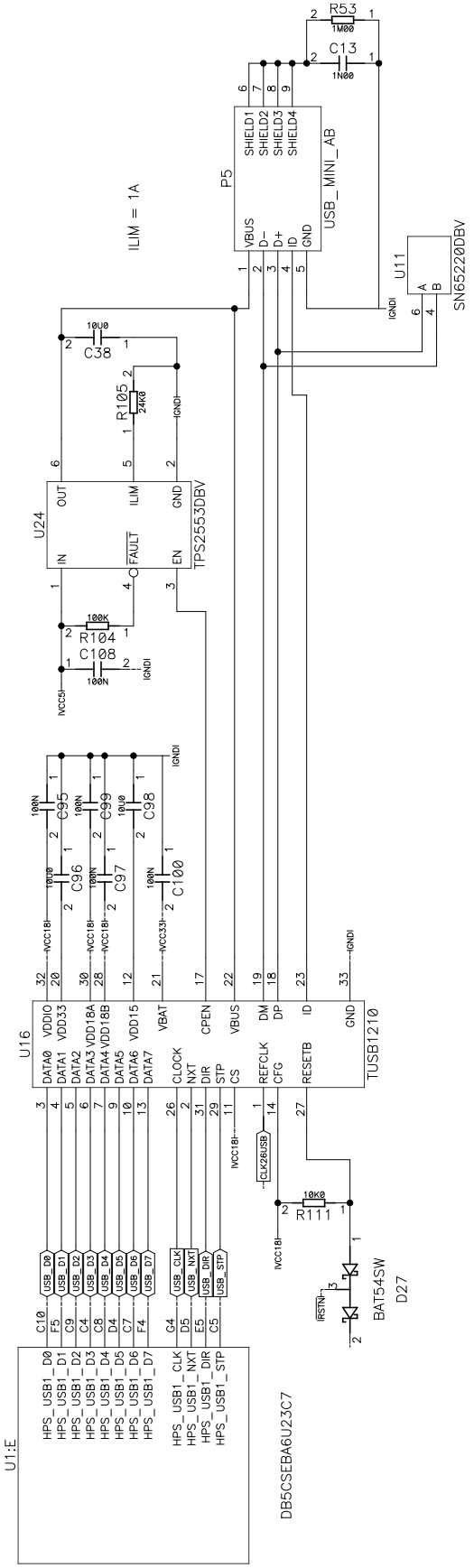
HPS : CAN, UART, RTC, Button, LEDs



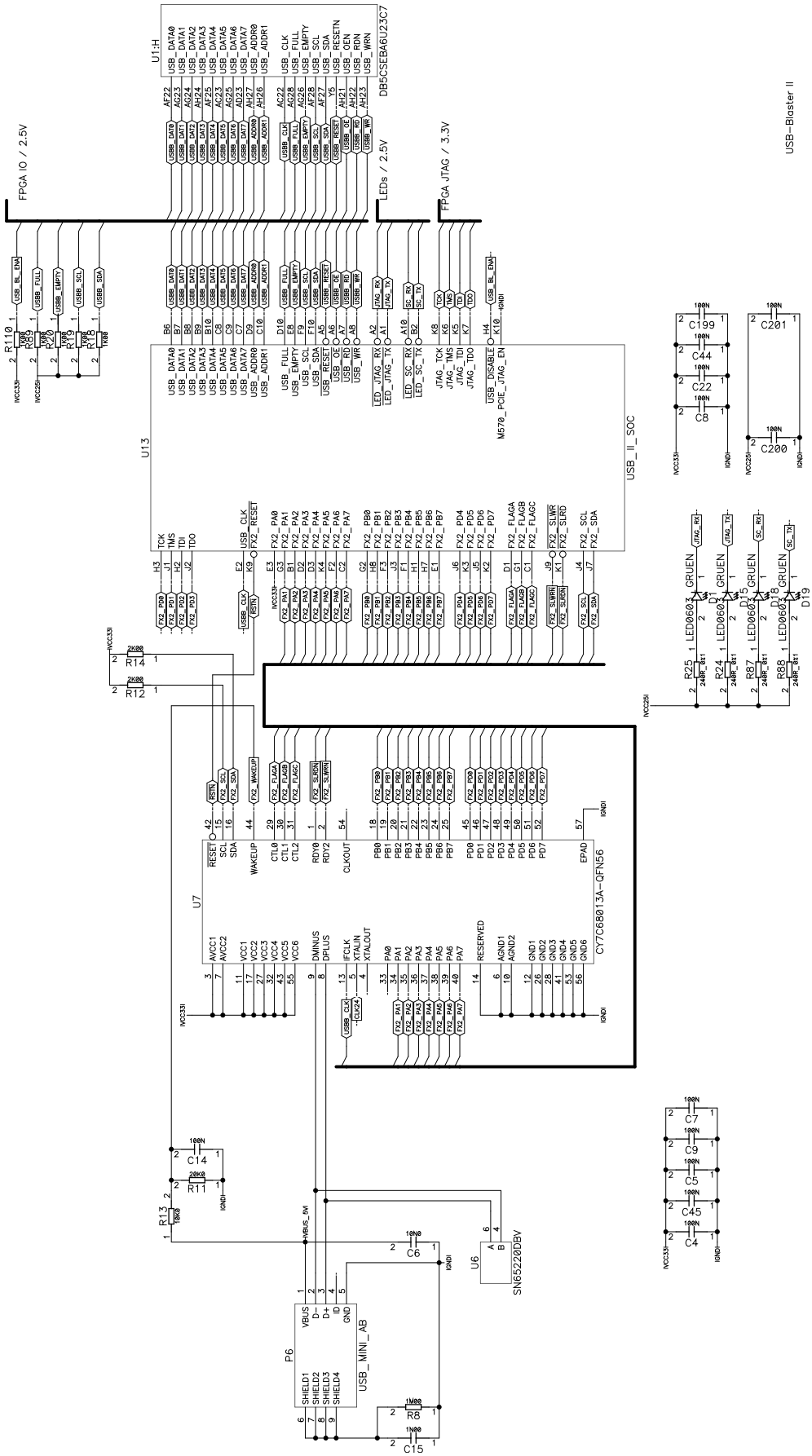
HPS : Gigabit Ethernet Phy



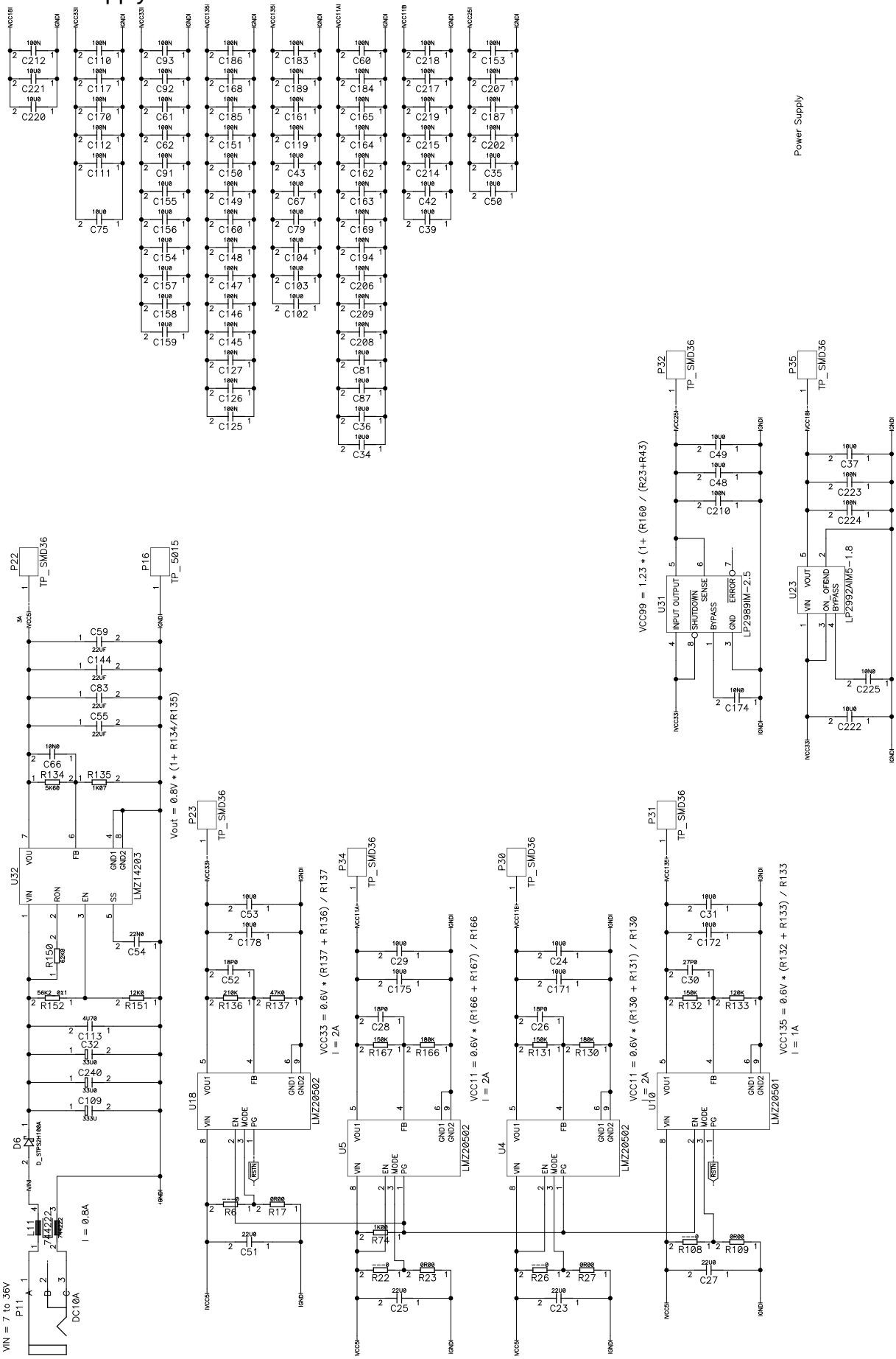
HPS : USB


R53
1M00
C13
1N00
P5
SHIELD1
SHIELD2
SHIELD3
SHIELD4
VBUS
D-
D+
ID
GND
USB_MINI_AB
ILIM = 1A
U11
SN65220DBV
C38
10U0
R105
24K0
U24
OUT
ILIM
GND
IN
FAULT
EN
TPS2553DBV
R104
100K
C108
100N
C95
C96
C99
C97
C98
C100
U16
VDDIO
VDD33
VDD18A
VDD18B
VDD15
VBAT
CPEN
VBUS
DM
DP
ID
GND
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
CLOCK
NXT
DIR
STP
CS
REFCLK
CFG
RESETB
TUSB1210
R111
10K0
BAT54SW
D27
U1:E
DB5CSEBA6U23C7
HPS_USB1_D0
HPS_USB1_D1
HPS_USB1_D2
HPS_USB1_D3
HPS_USB1_D4
HPS_USB1_D5
HPS_USB1_D6
HPS_USB1_D7
HPS_USB1_CLK
HPS_USB1_NXT
HPS_USB1_DIR
HPS_USB1_STP

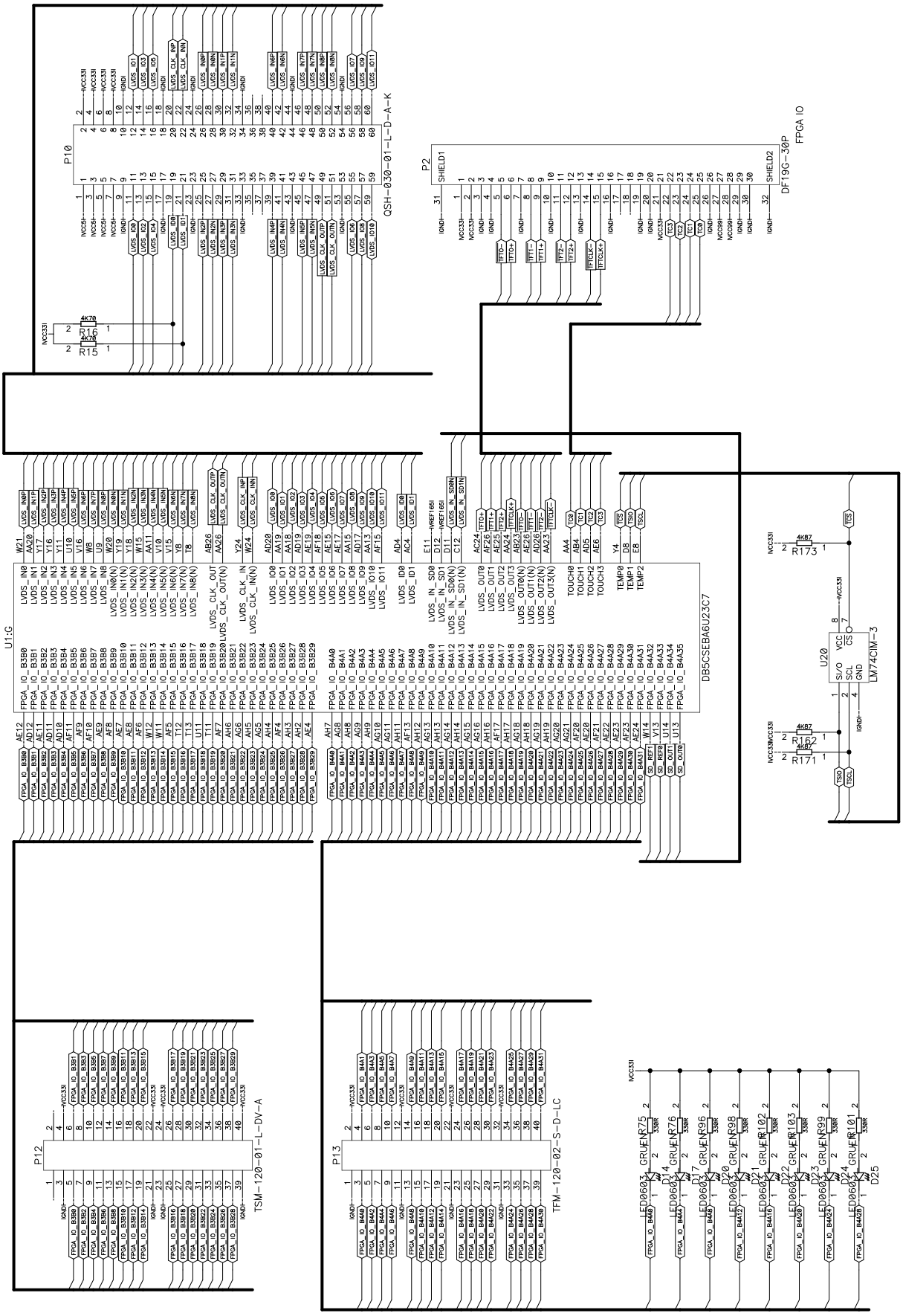
Embedded USB-Blaster II



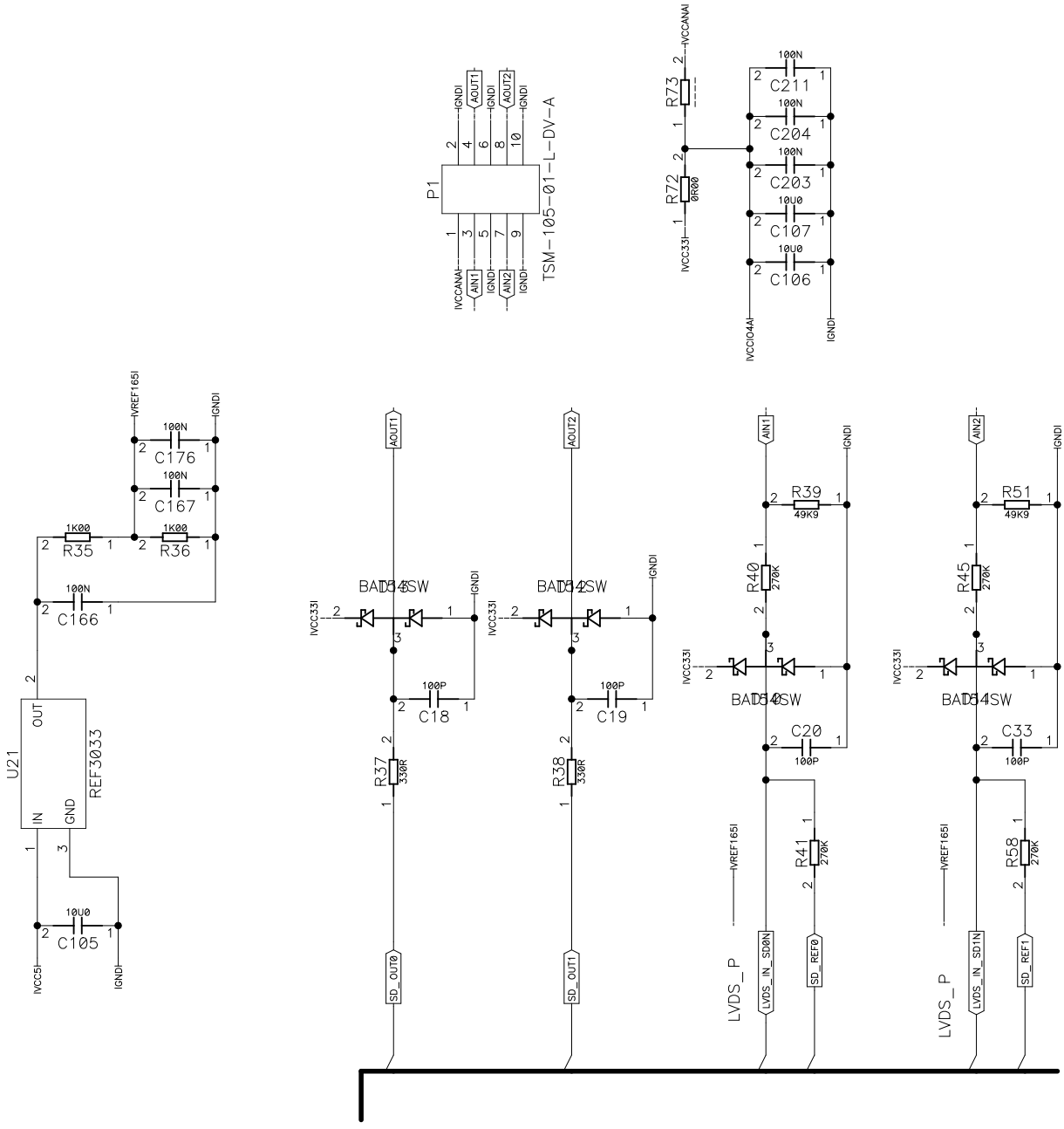
Power Supply



FPGA IO


P10
QSH-030-01-L-D-A-K
P2
SHIELD1
SHIELD2
DF19G-36P
FPGA IO
U1:G
DB5CSEBA6U23C7
P12
TSM-120-01-L-DV-A
P13
TFM-120-02-S-D-LC
U20
LM74CIM-3
R173
R162
R171
R15
R16
LED0603
GRUENR75
GRUENR76
GRUENR96
GRUENR98
GRUENR102
GRUENR103
GRUENR99
GRUENR101
D14
D17
D20
D21
D22
D23
D24
D25

SD-ADC / DAC Subsystem



Board Top View

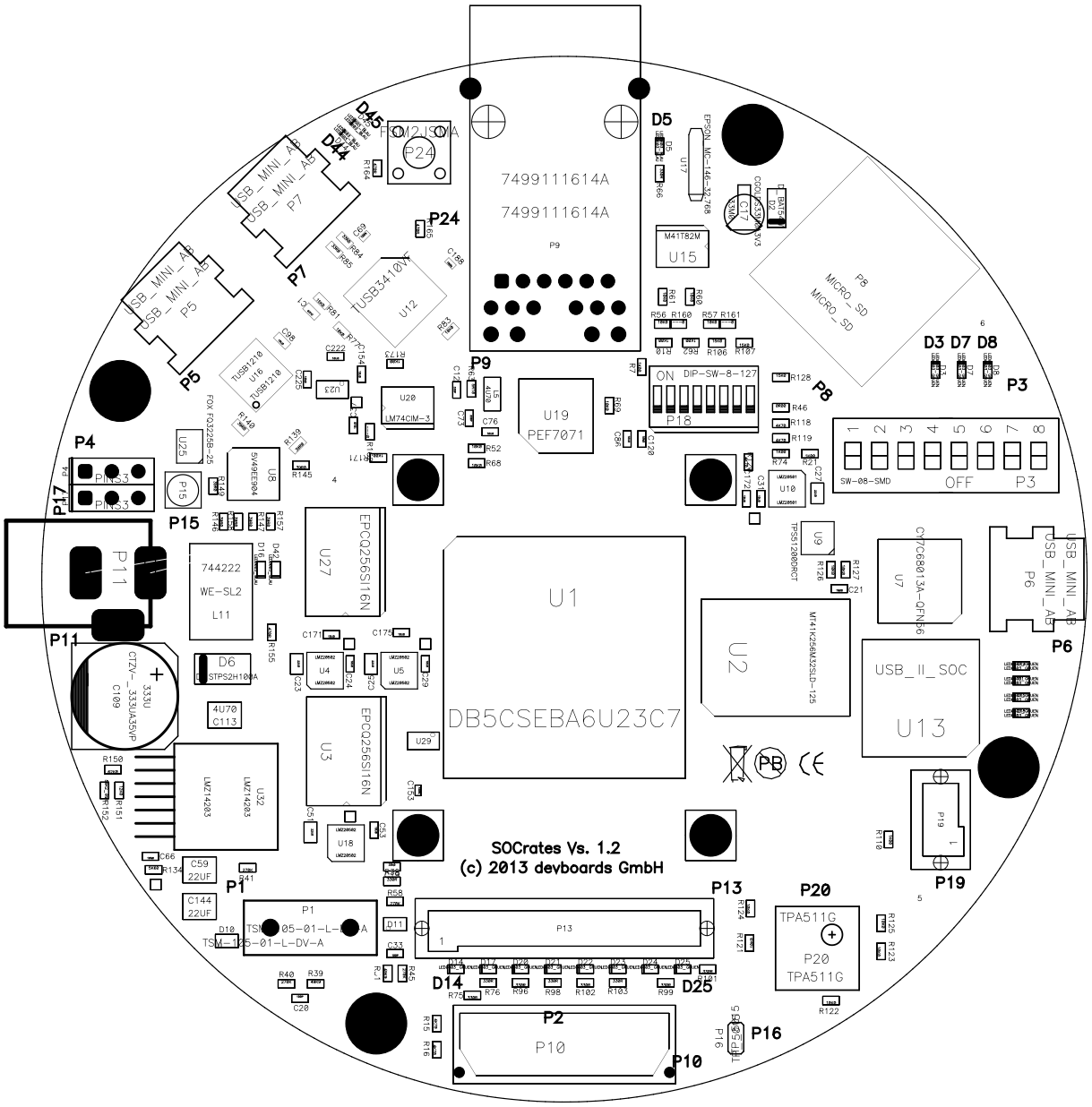


Figure 7

Board Bottom View

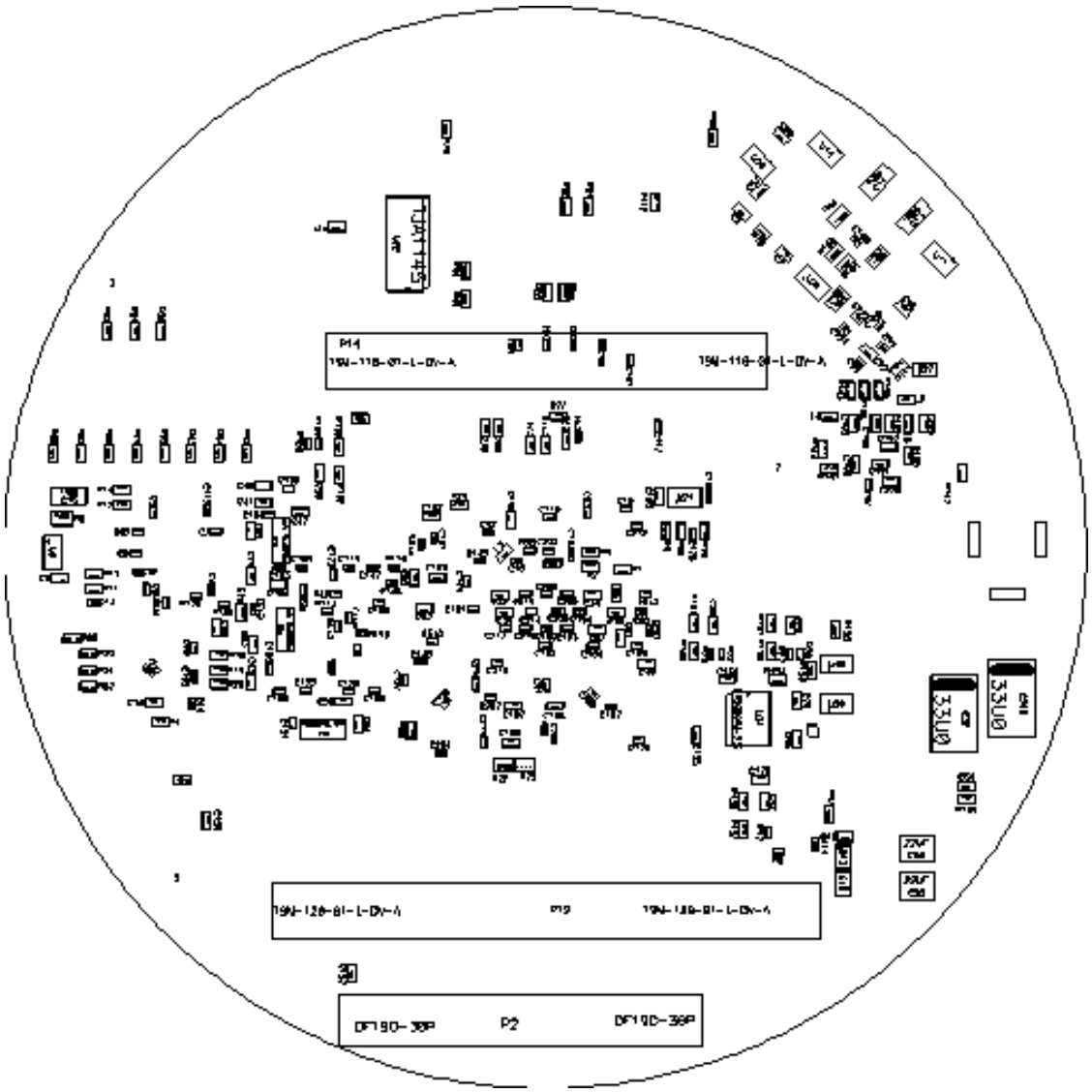


Figure 8

SoCrates-Phy1

The SoCrates-Phy1 add-on board builds a Dual 10/100 Ethernet Phy interface used for "Industrial Fieldbus" applications. The board is equipped with two TLK105 Ethernet Phys from Texas Instruments, an Access-IP CPLD, EEPROM and Atmel Security Device. The Phys are connected to the FPGA using the RMII standard.

Altera provides the use of industrial Ethernet protocols in a very easy way. Customer can buy an Access-IP licence and can use the "Real Time Ethernet Protocol" in the connected FPGA. The following Industrial Ethernet Protocols are available:

- Profibus
- Ethernet-IP
- Modbus TCP/IP
- Ethernet Powerlink
- Profinet

The Access-IP CPLD is implemented on the SoCrates-Phy1 add-on board. More information how to implement the respective fieldbusses can be found at www.altera.com/industrialethernet.

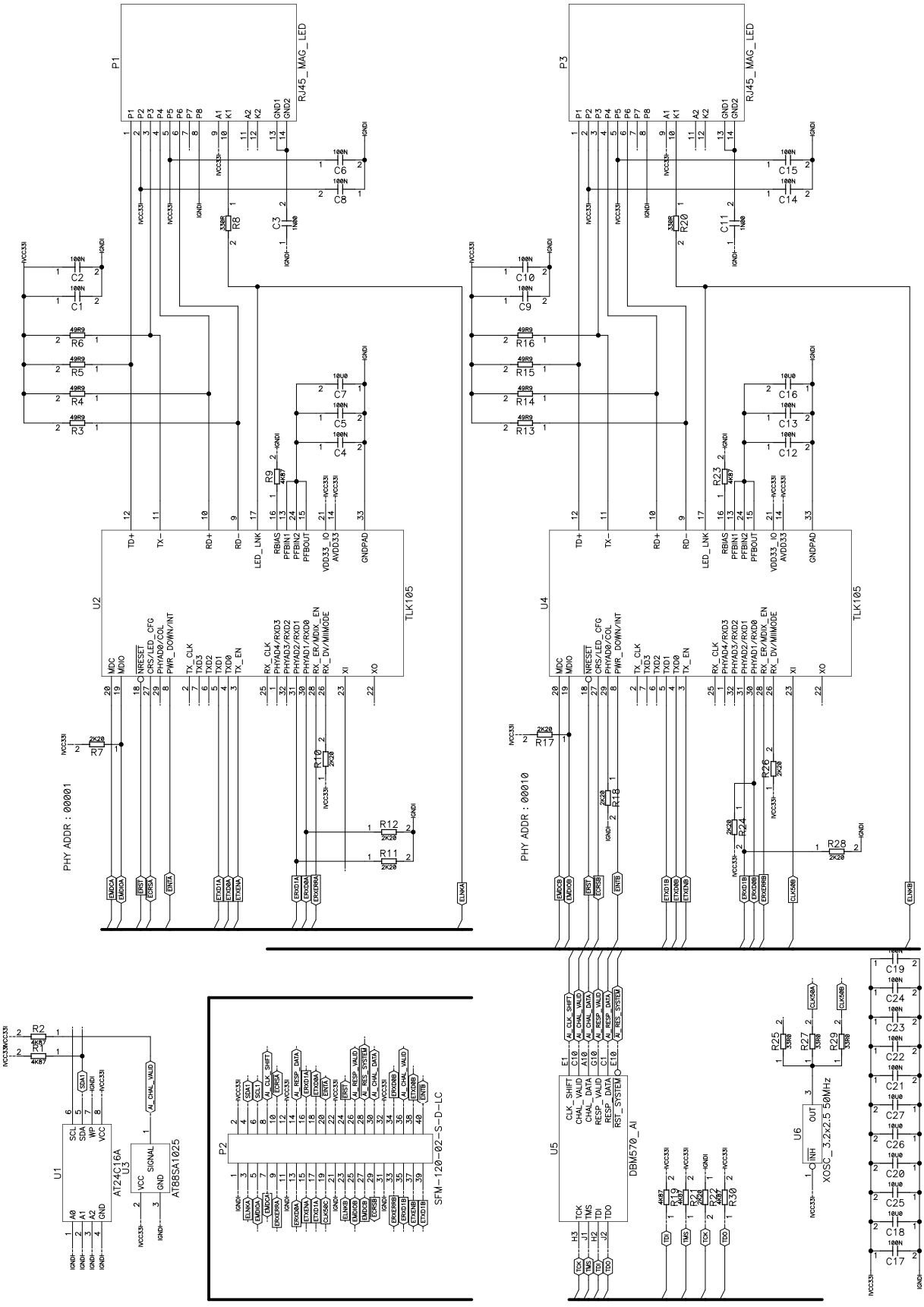
Dimension: 44 x 50mm

The SoCrates_Phy1 module can be mounted to SoCrates using the P13 connector.

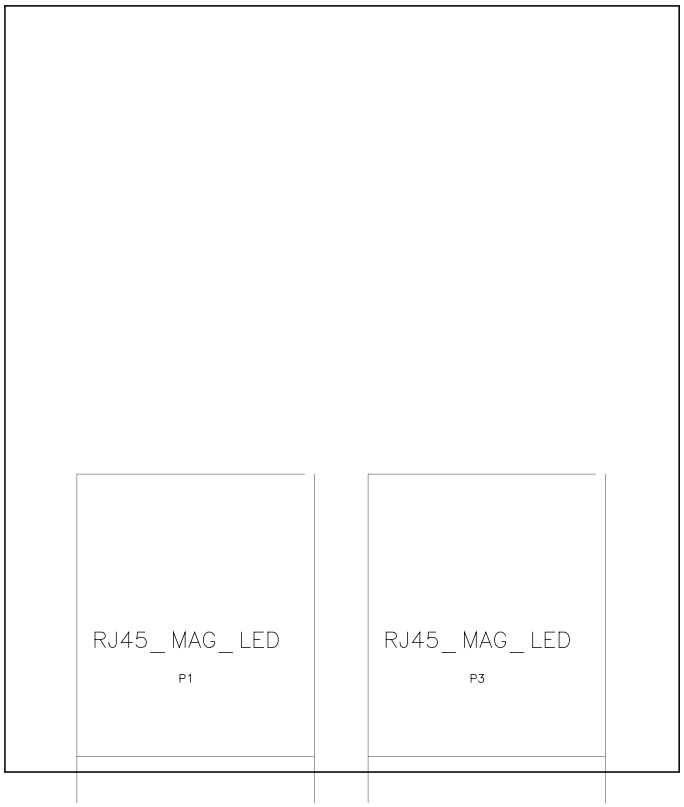
Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		VCC33
ELNKA	AH7	3	4	AG8	SDA1
EMDIOA	AH8	5	6	AG9	SCL1
EMDC	AH9	7	8	AG10	AI_CLK_SHIFT
ERXERRA	AG11	9	10	AH11	ECRSAn
GND		11	12		VCC33
ERXDA0	AF13	13	14	AH12	AI_RESP_DATA
ETXENA	AG13	15	16	AH13	ERXD1A
ETXD1A	AG14	17	18	AH14	ETXD0A
CLK50	AG15	19	20	AG16	EINTAn
GND		21	22		VCC33
ELNKB	AH16	23	24	AF17	ERSTn
EMDIOB	AH17	25	26	AG18	AI_RSP_VALID
EMDCB	AH18	27	28	AG19	AI_RES_SYSTEMn
ECRSBn	AH19	29	30	AG20	AI_CHAL_DATA
GND		31	32		VCC33
ERXERRB	AG21	33	34	AF20	ERXD0B
ERXD1B	AE20	35	36	AF21	AI_CHAL_VALID
ETXENB	AE22	37	38	AE23	ETXD0B
ETXD1B	AF23	39	40	AE24	EINTBn

Table 29

SoCrates-Phy1 Schematic



SoCrates-Phy1 Silk Top



SoCrates-Phy1 Silk Bottom